

Octal inverting buffer

74F240

FEATURES

- Octal bus interface
- 3-state buffer outputs sink 64 mA
- 15 mA source current

DESCRIPTION

The 74F240 is an octal inverting buffer that is ideal for driving bus lines of buffer memory address registers. The outputs are all capable of sinking 64 mA and sourcing up to 15 mA. The device features two output enables, each controlling four of the 3-state outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F240	4.3 ns	37 mA

ORDERING INFORMATION

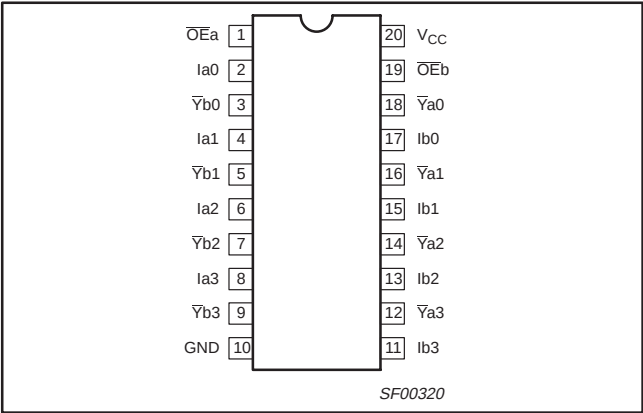
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V _{CC} = 5 V ±10%, T _{amb} = 0 °C to +70 °C	
20-pin plastic DIP	N74F240N	SOT146-1
20-pin plastic SOL	N74F240D	SOT163-1
20-pin plastic SSOP II	N74F240DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

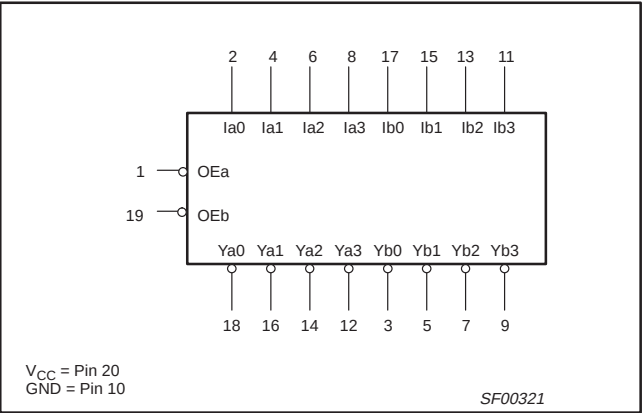
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I _{an} , I _{bn}	Data inputs	1.0/1.67	20 μA/1.0 mA
OE _a , OE _b	Output enable inputs (Active-LOW)	1.0/0.33	20 μA/0.2 mA
Y _{an} , Y _{bn}	Data outputs	750/106.7	15 mA/64 mA

Note to input and output loading and fan out table
One (1.0) FAST unit load is defined as: 20 μA in the HIGH state and 0.6 mA in the LOW state.

PIN CONFIGURATION



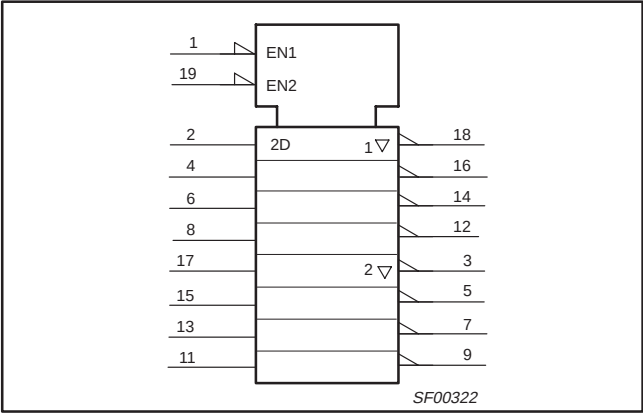
LOGIC SYMBOL



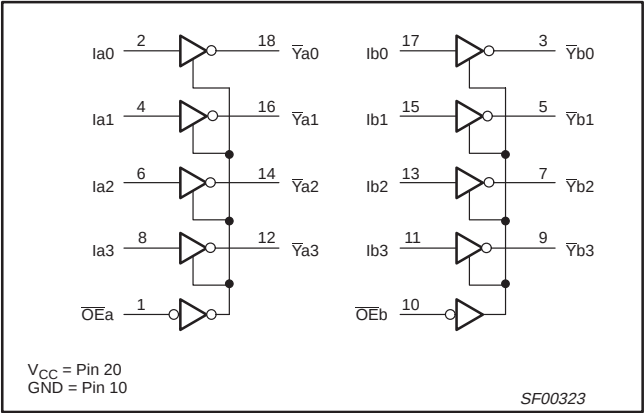
Octal inverting buffer

74F240

IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	$\overline{Y}a$	$\overline{Y}b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	128	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free air temperature range	0		+70	°C

Octal inverting buffer

74F240

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹		LIMITS			UNIT	
					MIN	TYP ²	MAX		
V _{OH}	High-level output voltage		V _{CC} = MIN; V _{IL} = MAX; V _{IH} = MIN	I _{OH} = −3 mA	±10%V _{CC}	2.4			V
					±5%V _{CC}	2.7	3.4		V
				I _{OH} = −15 mA	±10%V _{CC}	2.0			V
					±5%V _{CC}	2.0			V
V _{OL}	Low-level output voltage		V _{CC} = MIN; V _{IL} = MAX; V _{IH} = MIN	I _{OL} = MAX	±10%V _{CC}			0.50	V
					±5%V _{CC}		0.42	0.50	V
V _{IK}	Input clamp voltage		V _{CC} = MIN; I _I = I _{IK}			−0.73	−1.2		V
I _I	Input current at maximum input voltage		V _{CC} = MAX; V _I = 7.0 V					100	μA
I _{IH}	High-level input current		V _{CC} = MAX; V _I = 2.7 V					20	μA
I _{IL}	Low-level input current		V _{CC} = MAX; V _I = 0.5 V					−1.0	mA
I _{OZH}	Off-state output current, high-level voltage applied		V _{CC} = MAX, V _O = 2.7 V					50	μA
I _{OZL}	Off-state output current, low-level voltage applied		V _{CC} = MAX, V _O = 0.5 V					−50	μA
I _{OS}	Short-circuit output current ³		V _{CC} = MAX		−100			−225	mA
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX			12	18		mA
		I _{CCL}				50	70		mA
		I _{CCZ}				35	45		mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5 \text{ V}$, $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Octal inverting buffer

74F240

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25 °C V _{CC} = +5.0 V C _L = 50 pF; R _L = 500 Ω			T _{amb} = 0 °C to +70 °C V _{CC} = +5.0 V ± 10% C _L = 50 pF; R _L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay I _{an} , I _{bn} to $\bar{Y}_n$	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 2.0	7.5 5.0	ns
t _{PZH} t _{PZL}	Output enable time to high or low level	Waveform 2 & 3	3.0 4.5	5.0 6.5	7.5 8.5	3.0 4.0	9.0 10.0	ns
t _{PHZ} t _{PLZ}	Output disable time from high or low level	Waveform 2 & 3	3.0 3.0	5.5 5.0	7.0 7.0	3.0 3.0	7.5 7.5	ns

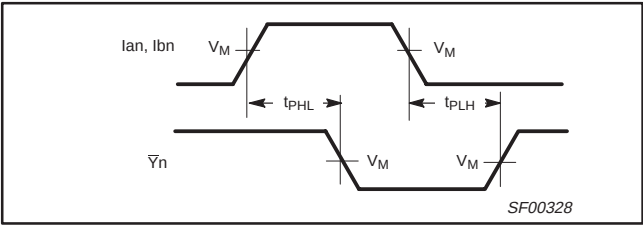
NOTES:

1. $|t_{pN} \text{ actual} - t_{pM} \text{ actual}|$ for any output compared to any other output where N and M are either LH or HL.

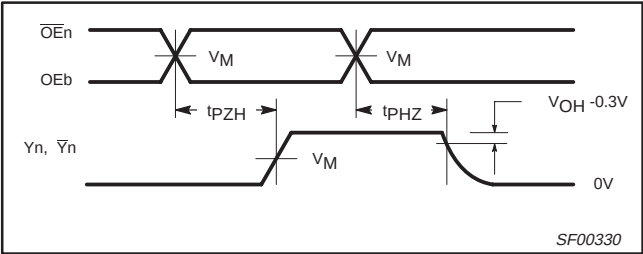
Octal inverting buffer

74F240

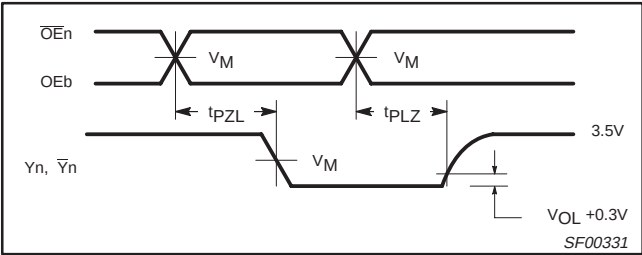
AC WAVEFORMS



Waveform 1. Propagation delay for inverting outputs



Waveform 2. 3-state output enable time to high level and output disable time from high level



Waveform 3. 3-state output enable time to low level and output disable time from low level

Notes to AC waveforms
1. For all waveforms, $V_M = 1.5\text{ V}$.

TEST CIRCUIT AND WAVEFORMS

Test Circuit for Open Collector Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:
 R_L = Load resistor; see AC electrical characteristics for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

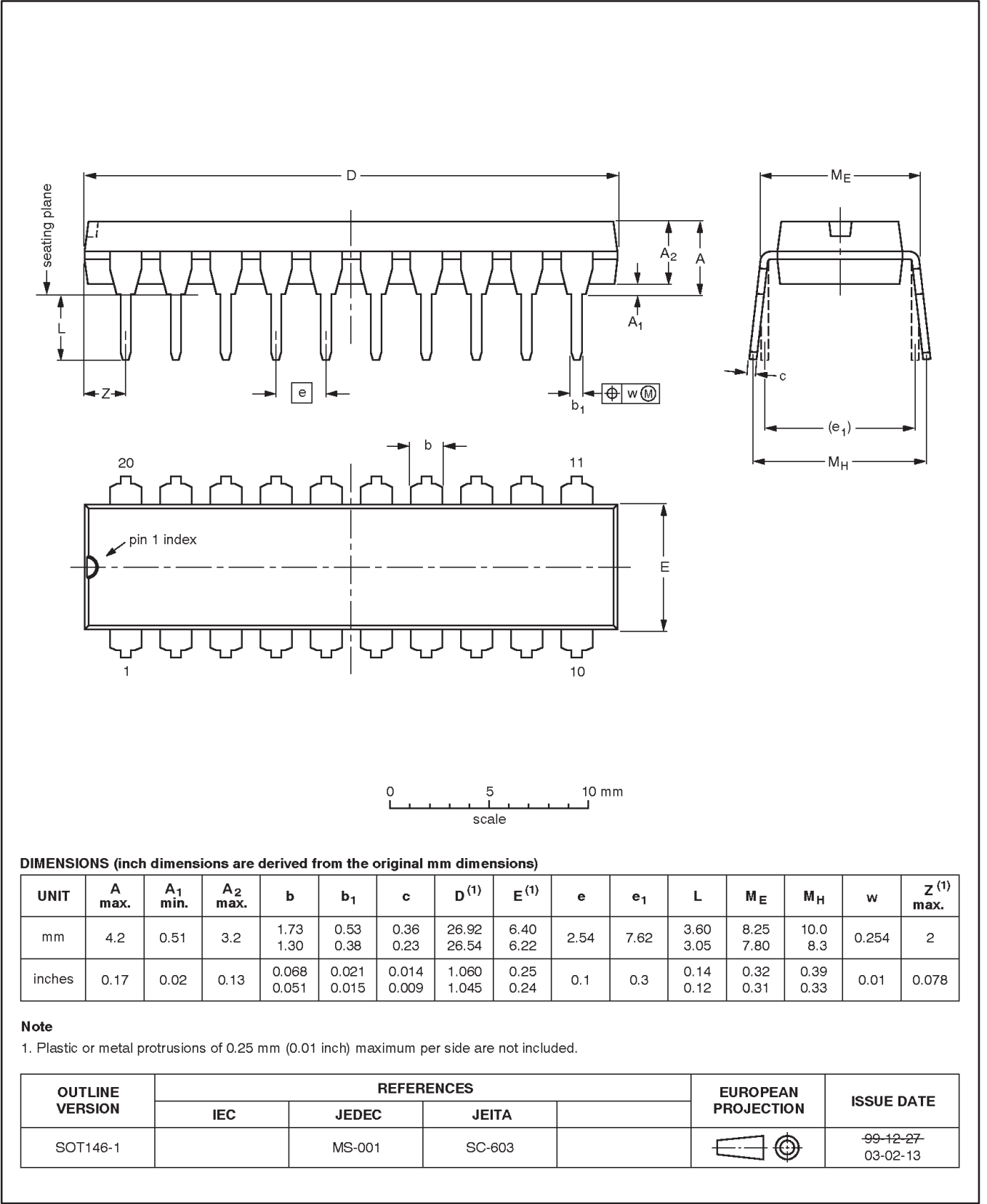
family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0 V	1.5 V	1 MHz	500 ns	2.5 ns	2.5 ns

Octal inverting buffer

74F240

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

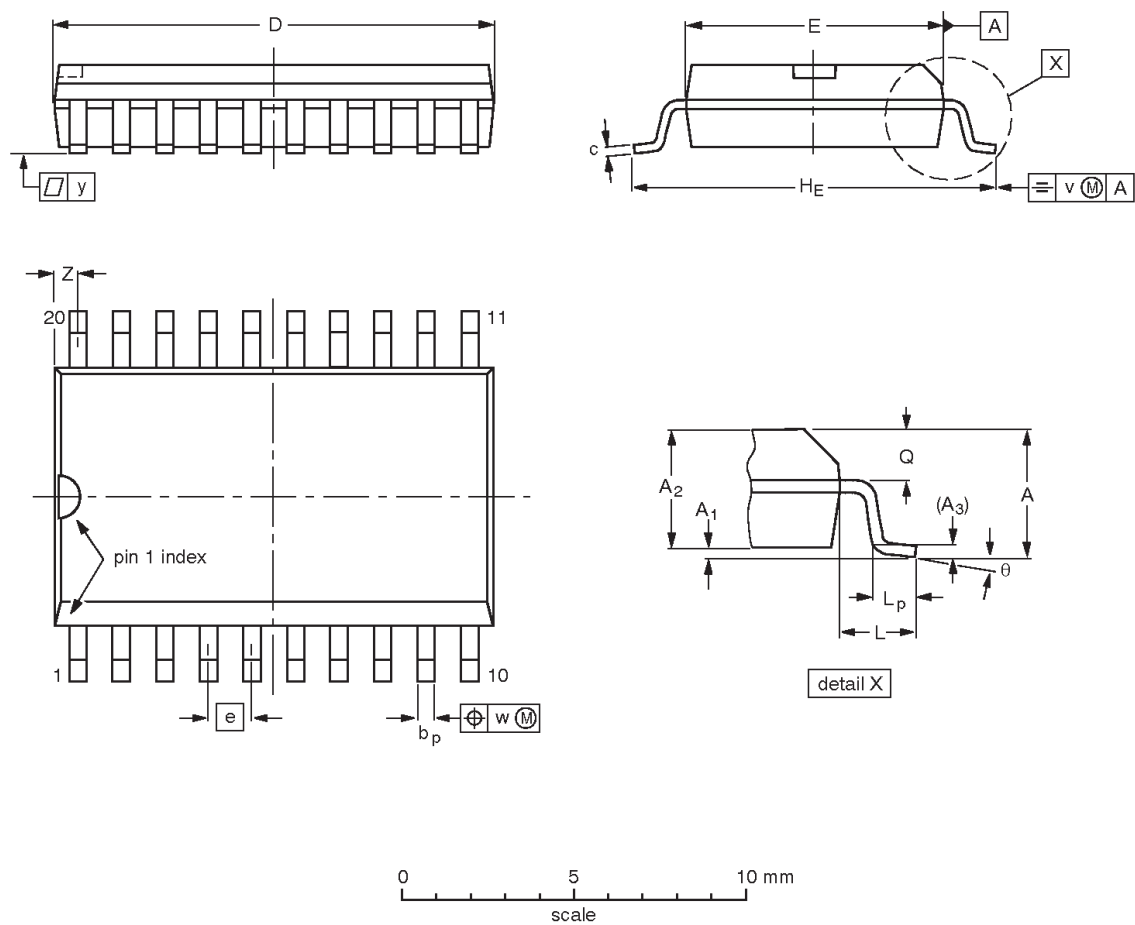


Octal inverting buffer

74F240

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				-99-12-27 03-02-19