

Buffers/Drivers

74F456

74F455 Octal Buffer/Driver with Parity, Inverting (3-State)
74F456 Octal Buffer/Driver with Parity, Non-Inverting (3-State)

FEATURES

- High impedance NPN base inputs for reduced loading (40µA in High and Low states)
- 74F456 combines 74F244 and 74F280A functions in one package
- 74F456 is a center pin version of the 74F656A
- 74F456 Non-Inverting
- 3-State outputs sink 64mA and source 15mA
- 24-pin plastic Slim DIP (300 mil) package
- Broadside pinout simplifies PC board layout

DESCRIPTION

The 74F455 and 74F456 are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F455	6.5ns	64mA
74F456	7.5ns	64mA

ORDERING INFORMATION

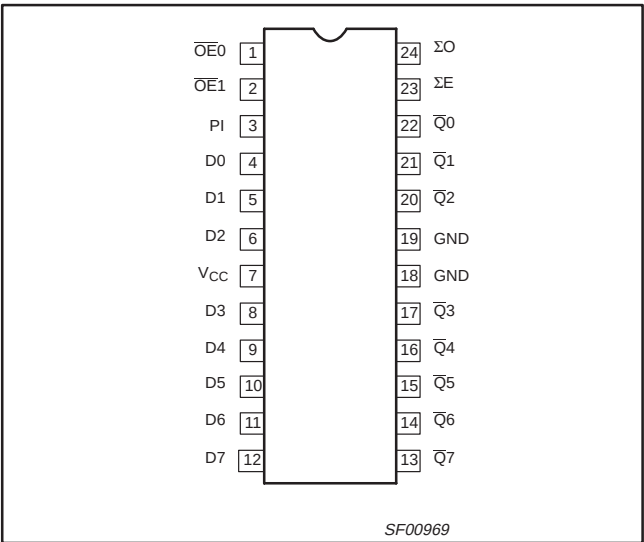
DESCRIPTION	COMMERCIAL RANGE V _{CC} = 5V ±10%, T _{amb} = 0°C to +70°C	PKG DWG #
24-pin plastic Slim DIP (300mil)	N74456N	SOT222-1
24-pin plastic SOL	N74456D	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

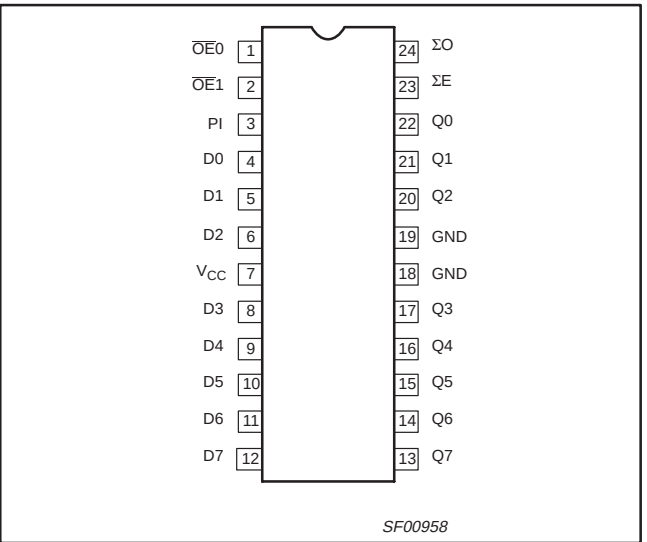
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D7	Data inputs	2.0/0.066	40µA/40µA
PI	Parity input	1.0/0.033	20µA/20µA
$\overline{OE}0$, $\overline{OE}1$	Output Enable inputs (active Low)	1.0/0.033	20µA/20µA
ΣE , ΣO	Parity outputs	750/106.7	15mA/64mA
$\overline{Q}0$ – $\overline{Q}7$	Data outputs (75F455)	750/106.7	15mA/64mA
Q0–Q7	Data outputs (75F456)	750/106.7	15mA/64mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION – 74F455



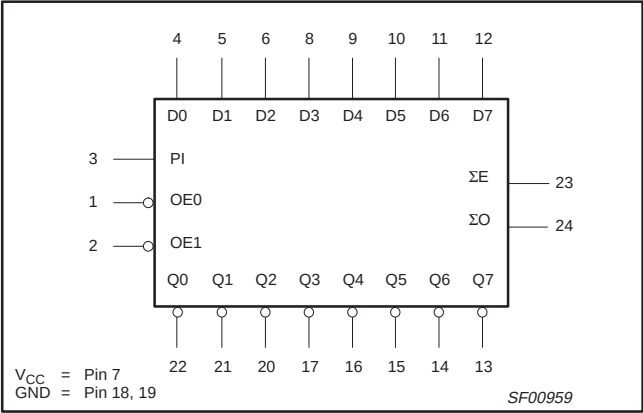
PIN CONFIGURATION – 74F456



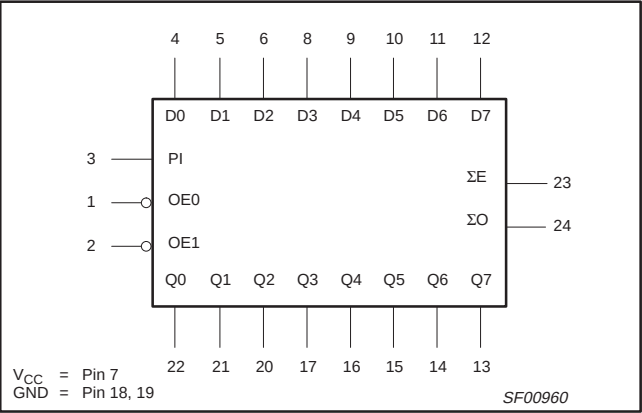
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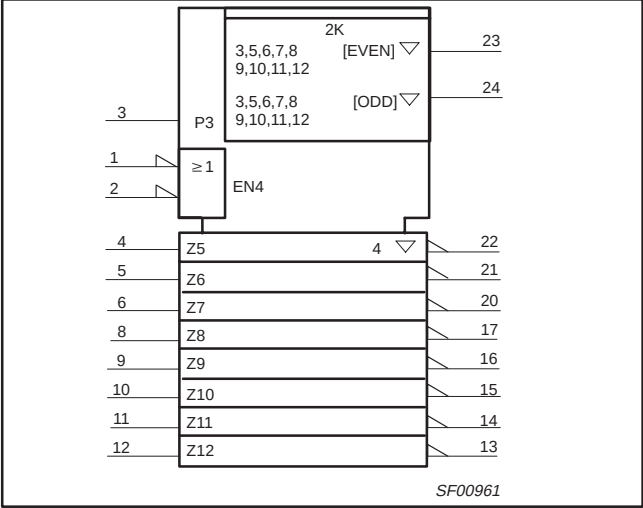
LOGIC SYMBOL – 74F455



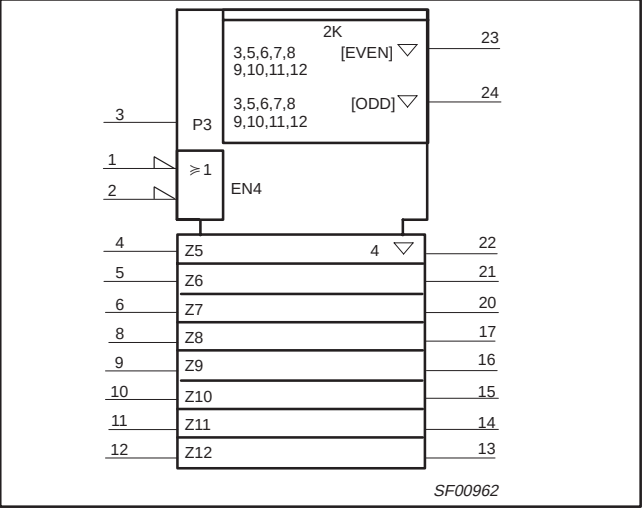
LOGIC SYMBOL – 74F456



LOGIC SYMBOL (IEEE/IEC) – 74F455



LOGIC SYMBOL (IEEE/IEC) – 74F456



FUNCTION TABLE

INPUTS			OUTPUTS	
			74F455	74F456
OE0	OE1	Dn	Qn	Qn
L	L	L	H	L
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance "off" state
X = Don't care

FUNCTION TABLE for PARITY OUTPUTS

INPUTS	OUTPUTS	
Number of inputs, High (PI, D0 - D7)	ΣE	ΣO
Even - 0, 2, 4, 6, 8	H	L
Odd - 1, 3, 5, 7, 9	L	H
Any OE _n = High	Z	Z

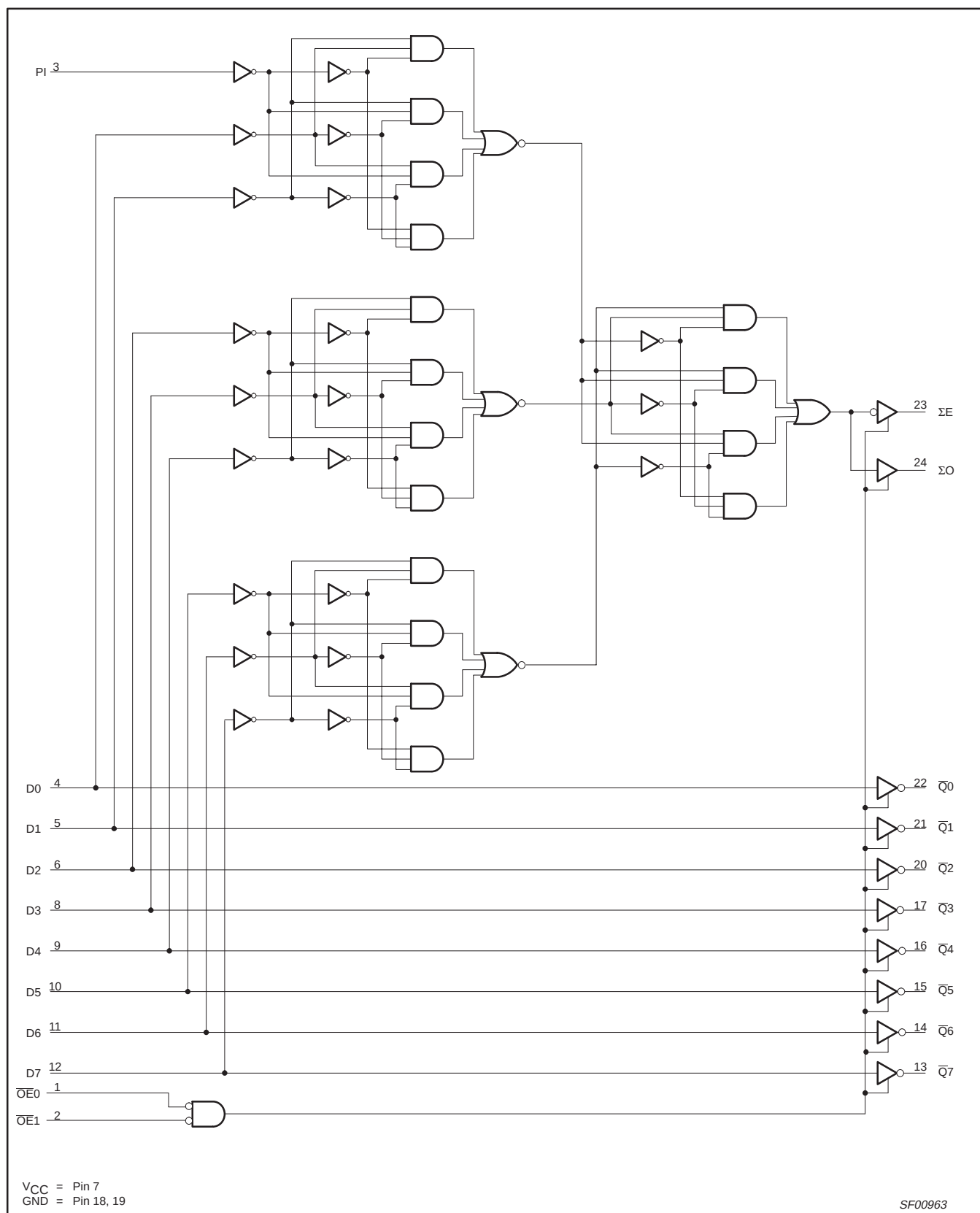
H = High voltage level
L = Low voltage level
Z = High impedance "off" state
X = Don't care

* Discontinued part. Please see the Discontinued Products List.

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LOGIC DIAGRAM for 74F455

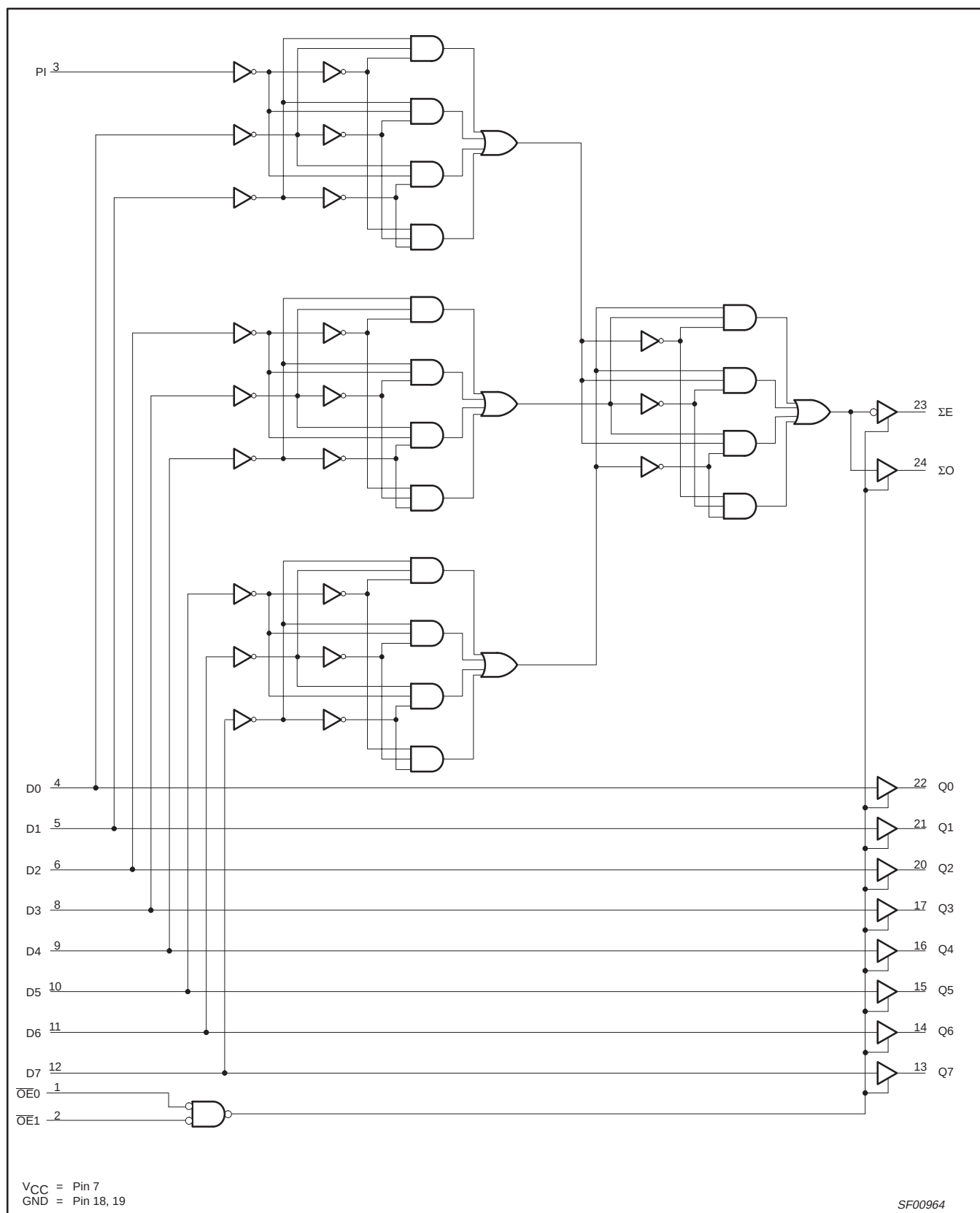


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LOGIC DIAGRAM for 74F456



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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.

Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	0		70	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			MIN	TYP ²	MAX	
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN I _{OH} = -3mA	±10%V _{CC}	2.4		V
			±5%V _{CC}	2.7	3.3	V
			I _{OH} = -15mA	±10%V _{CC}	2.0	V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN I _{OL} = MAX	±10%V _{CC}		0.55	V
			±5%V _{CC}	0.42	0.55	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}		-0.73	-1.2	V
I _I	Input current at maximum input voltage	V _{CC} = 0.0V, V _I = 7.0V			100	μA
I _{IH}	High-level input current	Dn PI, $\overline{OEn}$ V _{CC} = MAX, V _I = 4.7V			40	μA
					20	μA
I _{IL}	Low-level input current	Dn PI, $\overline{OEn}$ V _{CC} = MAX, V _I = 0.5V			-40	μA
					-20	μA
I _{OZH}	Off-state output current High-level voltage applied	V _{CC} = MAX, V _O = 2.7V			50	μA
I _{OZL}	Off-state output current Low-level voltage applied	V _{CC} = MAX, V _O = 0.5V			-50	μA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX	-100		-225	mA
I _{CC}	Supply current (total)	I _{CCH}		50	80	mA
		I _{CCL}		78	110	mA
		I _{CCZ}		63	90	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				V _{CC} = +5V T _{amb} = +25°C C _L = 50pF, R _L = 500Ω			V _{CC} = +5V ± 10% T _{amb} = 0°C to +70°C C _L = 50pF, R _L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay Dn to Qn	74F455	Waveform 2	2.0 1.0	4.5 2.0	6.5 4.0	2.0 1.0	7.5 4.5	ns
t _{PLH} t _{PHL}	Propagation delay Dn to Qn	74F456	Waveform 1	2.0 2.5	4.5 5.0	6.5 7.0	2.0 2.5	7.0 7.5	ns
t _{PLH} t _{PHL}	Propagation delay Dn to ΣE, ΣO		Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	ns
t _{PZH} t _{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	2.5 4.0	4.0 8.0	8.0 10.5	2.5 4.0	9.0 11.5	ns
t _{PHZ} t _{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	1.5 2.0	4.0 5.0	6.5 7.5	1.5 2.0	7.5 8.0	ns

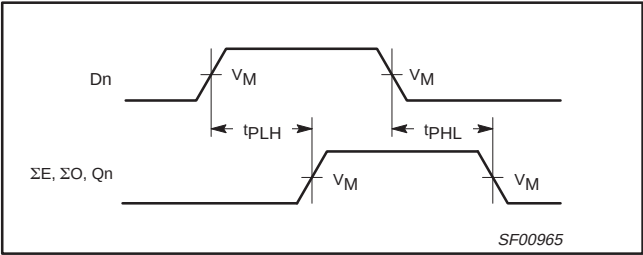
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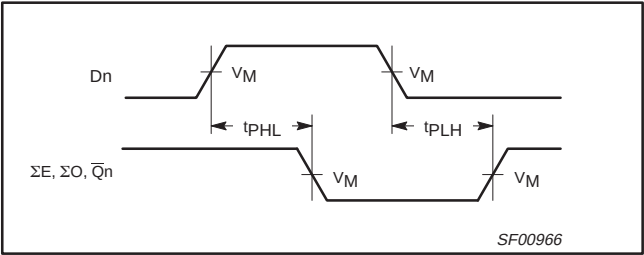
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AC WAVEFORMS

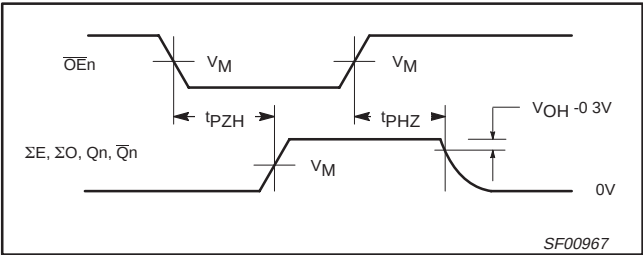
For all waveforms, $V_M = 1.5V$.



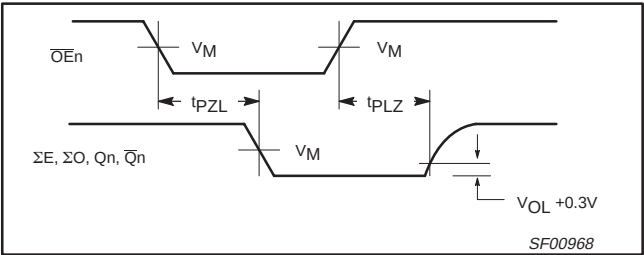
Waveform 1. Propagation Delay, Non-Inverting Outputs



Waveform 2. Propagation Delay, Inverting Outputs



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

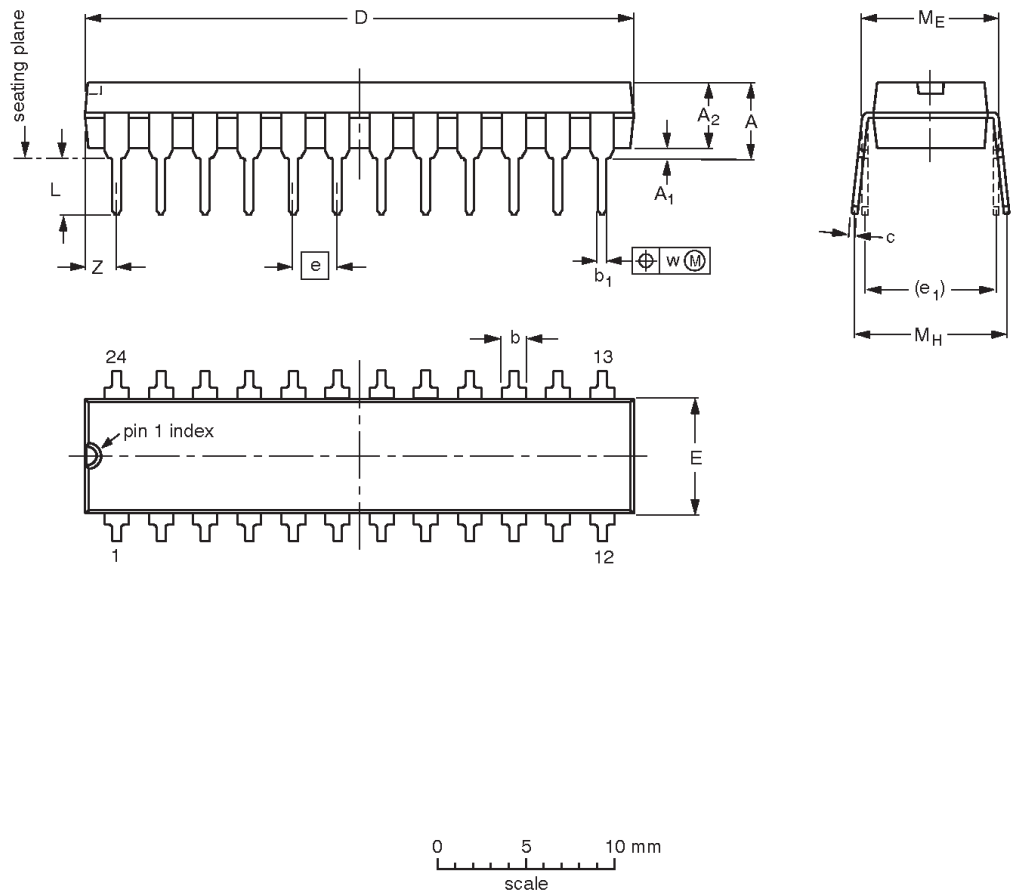
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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11