

1-of-10 decoder (3-State)

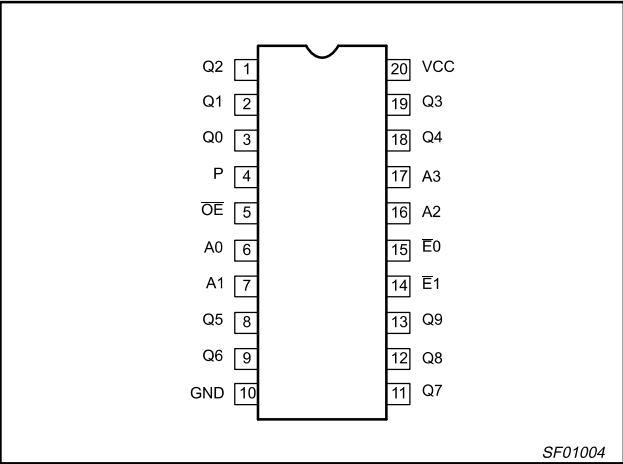
74F537

DESCRIPTION

The 74F537 is a one-of-ten decoder/demultiplexer with four active High BCD inputs and ten mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active Low or active High. The 74F537 has 3-State outputs and a High signal on the Output Enables ($\overline{OE}$) input forces all outputs to the high impedance state. Two input Enables, active High (E1) and active Low ($\overline{E0}$), are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine causes all outputs to go to the inactive state (i.e., same polarity as the P input).

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F537	9ns	44mA

PIN CONFIGURATION



ORDERING INFORMATION

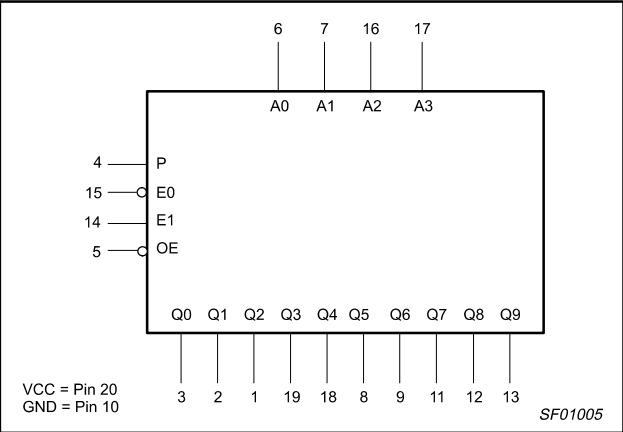
DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$
20-Pin Plastic DIP	N74F537N
20-Pin Plastic SOL	N74F537D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

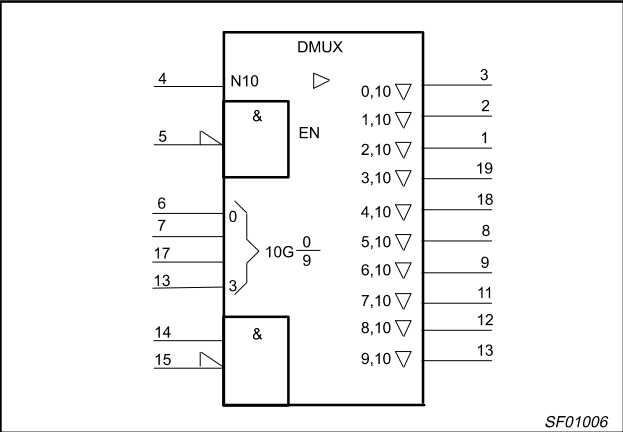
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A3	Data inputs	1.0/1.0	20 μ A/0.6mA
$\overline{E0}$	Enable input (active Low)	1.0/1.0	20 μ A/0.6mA
E1	Enable input (active High)	1.0/1.0	20 μ A/0.6mA
P	Polarity control input	1.0/1.0	20 μ A/0.6mA
$\overline{OE}$	Output Enable input	1.0/1.0	20 μ A/0.6mA
Q0 - Q9	Data outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



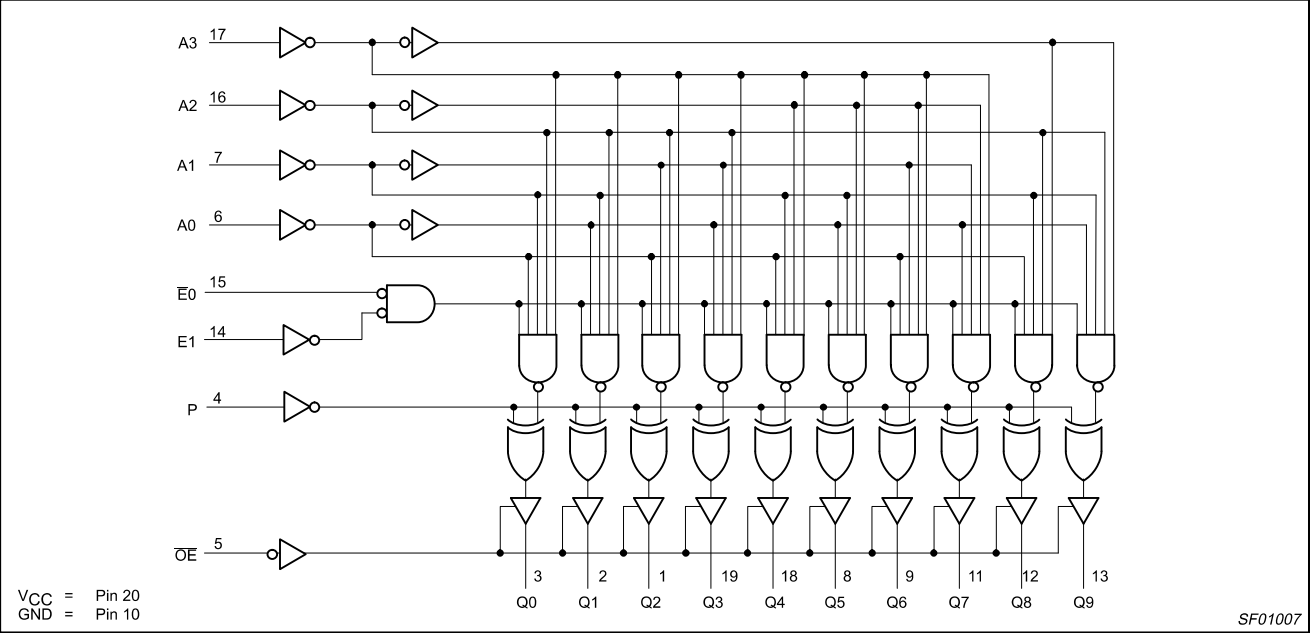
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS										OPERATING MODE
OE	E0	E1	A3	A2	A1	A0	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	
H	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	High Impedance
L	H	X	X	X	X	X	Outputs equal P input										Disable
L	X	L	X	X	X	X											
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	Active High output (P = L)
L	L	H	L	L	L	H	L	H	L	L	L	L	L	L	L	L	
L	L	H	L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	H	L	L	H	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	L	H	L	L	L	L	L	H	L	L	L	L	L	L	
L	L	H	L	H	L	H	L	L	L	L	H	L	L	L	L	L	
L	L	H	L	H	H	L	L	L	L	L	L	H	L	L	L	L	
L	L	H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	Active Low output (P = H)
L	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H	
L	L	H	L	L	H	L	H	H	L	H	H	H	H	H	H	H	
L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	
L	L	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	
L	L	H	L	H	H	L	H	H	H	H	H	L	H	H	H	H	
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3.0	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹		LIMITS			UNIT
				MIN	TYP ²	MAX	
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX	±10%V _{CC}	2.4			V
			±5%V _{CC}	2.7	3.3		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OL} = MAX	±10%V _{CC}		0.35	0.50	V
			±5%V _{CC}		0.35	0.50	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			−0.73	−1.2	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V				100	μA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V				20	μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5V				−0.6	mA
I _{OZH}	Off-state current High-level voltage applied	V _{CC} = MAX, V _O = 2.7V				50	μA
I _{OZL}	Off-state current Low-level voltage applied	V _{CC} = MAX, V _O = 0.5V				−50	μA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		−60		−150	mA
I _{CC}	Supply current (total)	V _{CC} = MAX			44	66	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

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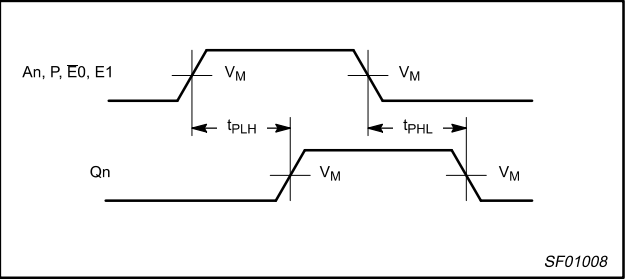
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AC ELECTRICAL CHARACTERISTICS

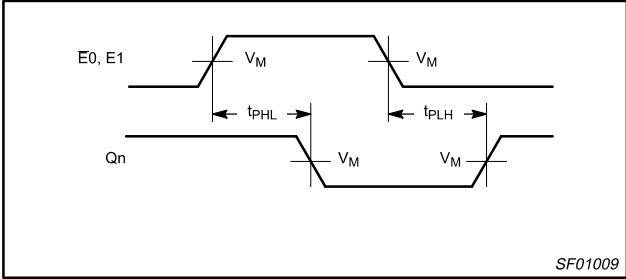
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay An to Qn	Waveform 1	4.5 3.0	9.0 7.5	14.0 11.0	4.5 3.0	16.0 12.0	ns ns
t _{PLH} t _{PHL}	Propagation delay E0 to Qn	Waveform 2	4.0 3.0	8.0 8.0	11.0 11.0	4.0 3.0	12.0 12.0	ns ns
t _{PLH} t _{PHL}	Propagation delay E1 to Qn	Waveform 2	6.0 4.0	8.5 8.5	11.5 11.5	6.0 4.0	13.0 12.5	ns ns
t _{PLH} t _{PHL}	Propagation delay P to Qn	Waveform 1	5.0 3.5	12.5 6.5	16.0 10.0	5.0 3.5	17.0 11.0	ns ns
t _{PZH} t _{PZL}	Output Enable time OE to Qn	Waveform 3 Waveform 4	2.5 4.0	4.5 5.5	7.0 8.0	2.5 4.0	8.0 9.0	ns ns
t _{PHZ} t _{PLZ}	Output Disable time OE to Qn	Waveform 3 Waveform 4	1.5 2.0	3.0 4.0	6.0 6.5	1.0 2.0	7.0 7.0	ns ns

AC WAVEFORMS

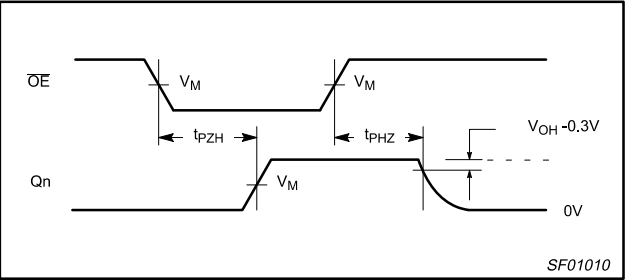
For all waveforms, V_M = 1.5V.



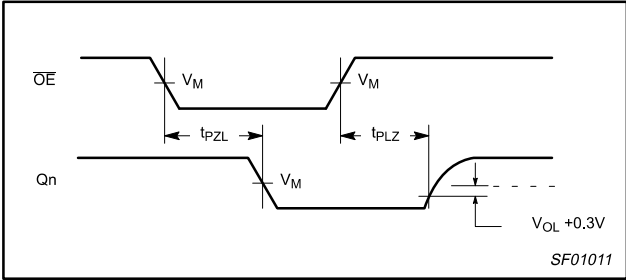
Waveform 1. Propagation Delay for Non-Inverting Outputs



Waveform 2. Propagation Delay for Inverting Outputs



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

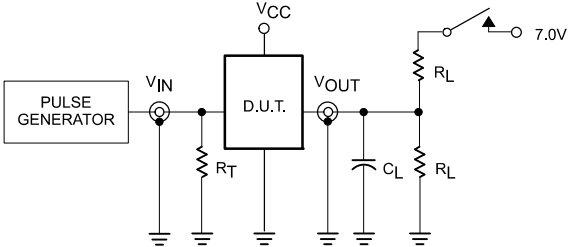


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

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TEST CIRCUIT AND WAVEFORM



The diagram shows a Pulse Generator connected to the input V_{IN} of a D.U.T. (Device Under Test). The input line has a termination resistor R_T to ground. The output V_{OUT} is connected to a load resistor R_L and a load capacitor C_L to ground. A switch is connected to the output line, controlled by a 7.0V signal. The supply voltage V_{CC} is connected to the top of the D.U.T.

Test Circuit for 3-State Outputs

SWITCH POSITION

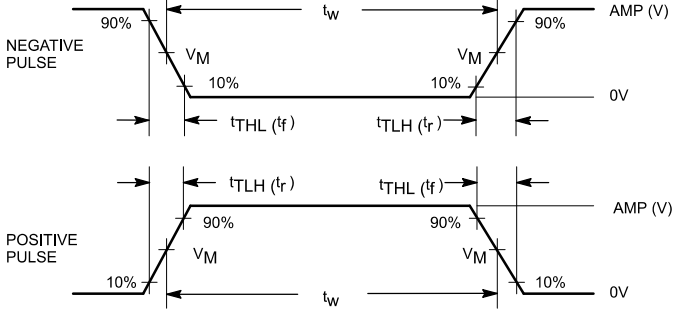
TEST	SWITCH
t_{PLZ}	closed
t_{pZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor;
see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



The waveforms show a Negative Pulse and a Positive Pulse. For the Negative Pulse, the signal transitions from 90% V_M to 10% V_M and back. The pulse width is t_w , and the transition times are $t_{TLH}(t_r)$ and $t_{THL}(t_f)$. For the Positive Pulse, the signal transitions from 10% V_M to 90% V_M and back. The pulse width is t_w , and the transition times are $t_{TLH}(t_r)$ and $t_{THL}(t_f)$. The voltage levels are marked as 90%, V_M , 10%, and 0V.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777