

Octal bus transceiver; 3-state; inverting

74HC/HCT640

FEATURES

- Octal bidirectional bus interface
- Inverting 3-state outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT640 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT640 are octal transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions.

The "640" features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated. The "640" is similar to the "245" but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to B_n ; B_n to A_n	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	9	9	ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	35	35	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

Octal bus transceiver; 3-state; inverting

74HC/HCT640

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₇	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B ₀ to B ₇	data inputs/outputs
19	$\overline{\text{OE}}$	output enable input (active LOW)
20	V _{CC}	positive supply voltage

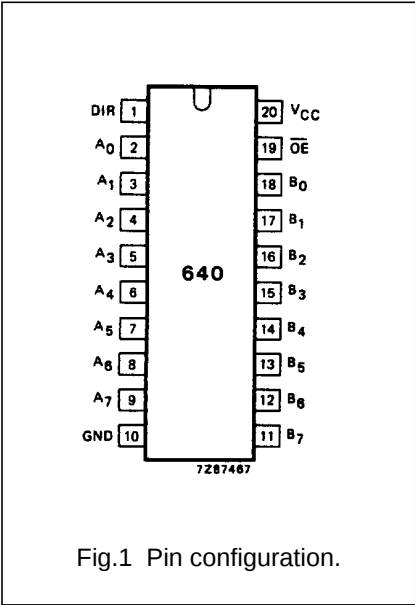


Fig.1 Pin configuration.

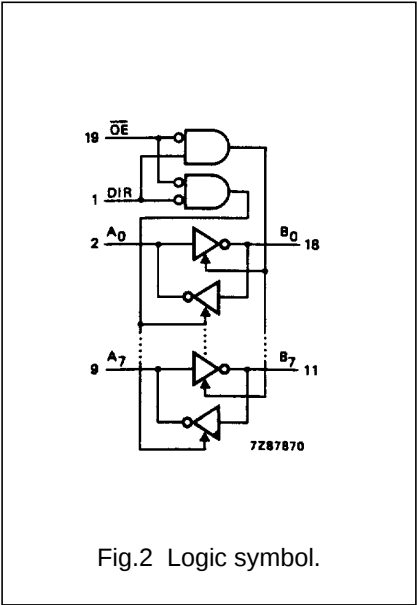


Fig.2 Logic symbol.

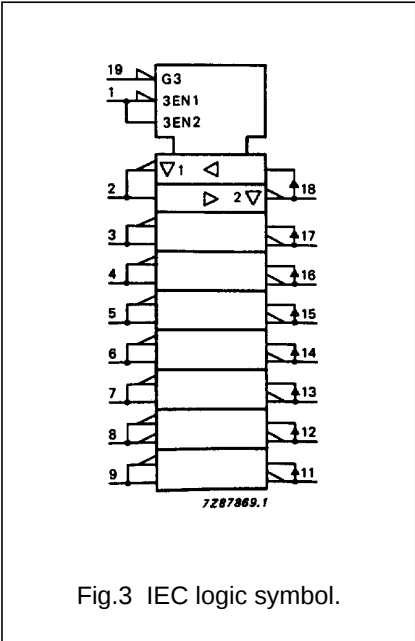


Fig.3 IEC logic symbol.

FUNCTION TABLE

inputs		inputs/outputs	
$\overline{\text{OE}}$	DIR	A _n	B _n
L	L	A = $\overline{\text{B}}$	inputs
L	H	inputs	B = $\overline{\text{A}}$
H	X	Z	Z

- Note
1. H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

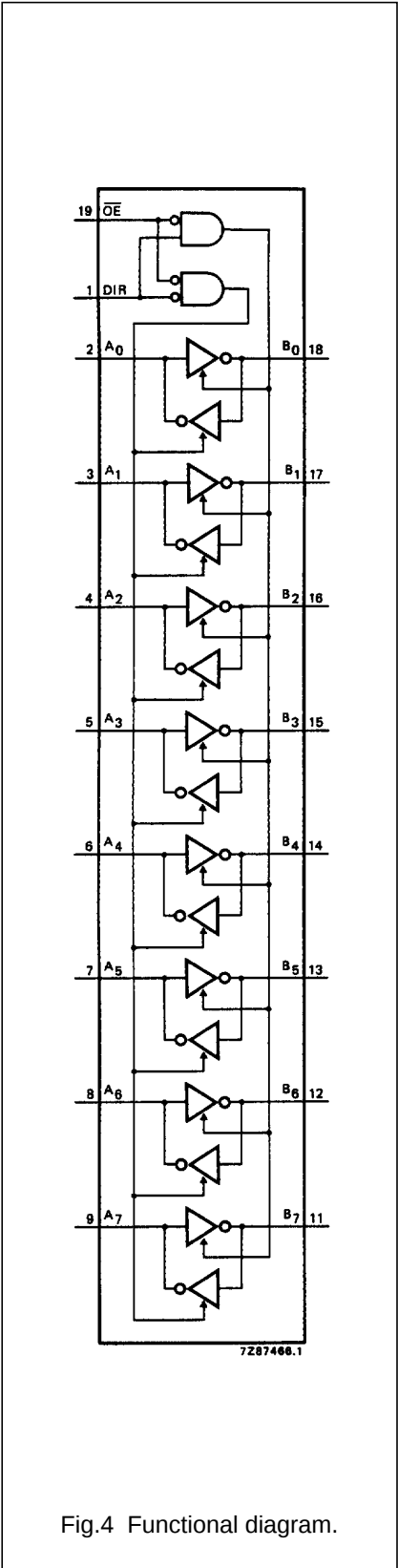


Fig.4 Functional diagram.

Octal bus transceiver; 3-state; inverting

74HC/HCT640

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to B _n ; B _n to A _n		30	90		115		135	ns	2.0	Fig.5
			11	18		23		27		4.5	
			9	15		20		23		6.0	
t _{PZH} / t _{PZL}	3-state output enable time $\overline{\text{OE}}$, DIR to A _n ; $\overline{\text{OE}}$, DIR to B _n		44	150		190		225	ns	2.0	Fig.6
			16	30		38		45		4.5	
			13	26		33		38		6.0	
t _{PHZ} / t _{PLZ}	3-state output disable time $\overline{\text{OE}}$, DIR to A _n ; $\overline{\text{OE}}$, DIR to B _n		50	150		190		225	ns	2.0	Fig.6
			18	30		38		45		4.5	
			14	26		33		38		6.0	
t _{THL} / t _{TLH}	output transition time		14	60		75		90	ns	2.0	Fig.5
			5	12		15		18		4.5	
			4	10		13		15		6.0	

Octal bus transceiver; 3-state; inverting

74HC/HCT640

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A _n	1.50
B _n	1.50
$\overline{OE}$	1.50
DIR	0.90

AC CHARACTERISTICS FOR 74HCT

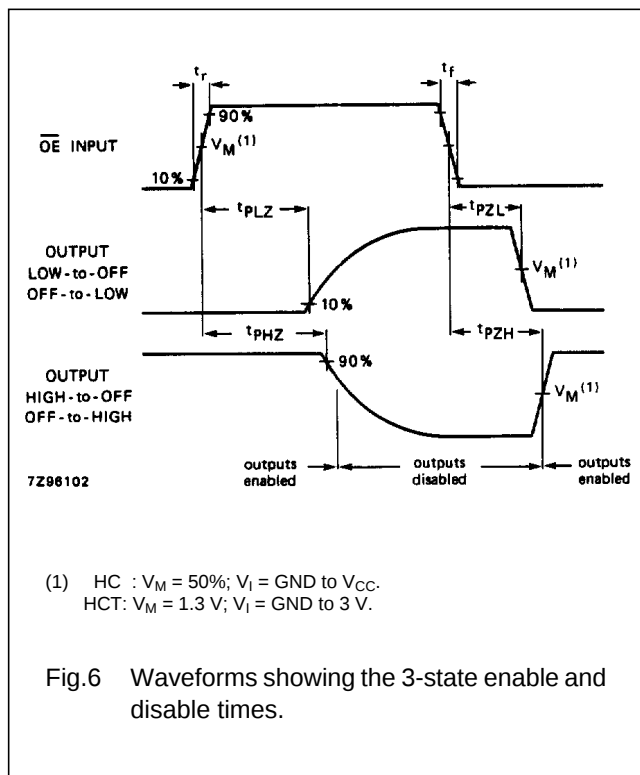
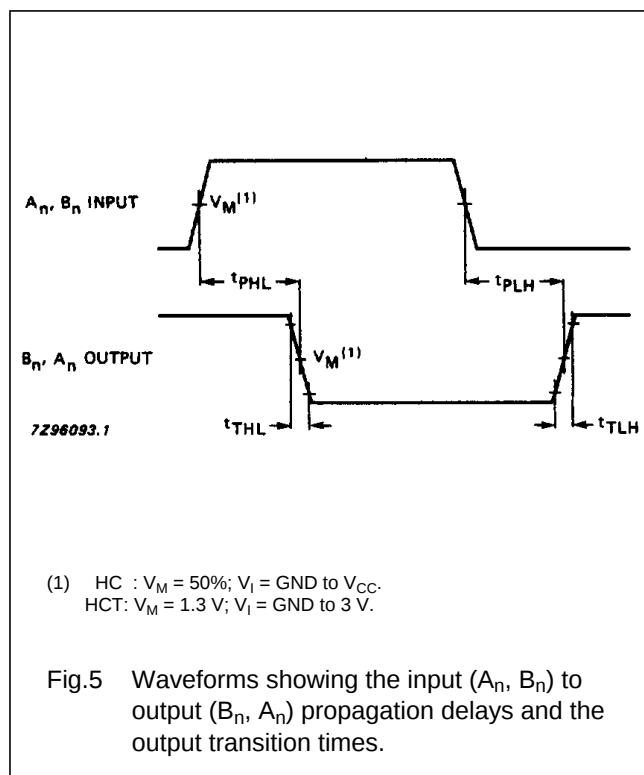
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to B _n ; B _n to A _n		11	22		28		33	ns	4.5	Fig.5
t _{PZH} / t _{PZL}	3-state output enable time $\overline{OE}$, DIR to A _n ; $\overline{OE}$, DIR to B _n		18	30		38		45	ns	4.5	Fig.6
t _{PHZ} / t _{PLZ}	3-state output disable time $\overline{OE}$, DIR to A _n ; $\overline{OE}$, DIR to B _n		19	30		38		45	ns	4.5	Fig.6
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.5

Octal bus transceiver; 3-state; inverting

74HC/HCT640

AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".