CD40208BMS

CMOS 4 x 4 Multiport Register

December 1992

Features

- High Voltage Types (20V Rating)
- One Input and Two Output Buses
- Unlimited Expansion in Bit and Word Directions
- Data Lines have Latched Inputs
- 3-State Outputs
- Separate Control of Each Bus, Allowing Simultaneous Independent Reading of any of Four Registers on Bus A and Bus B and Independent Writing Into any of the Four Registers
- 100% Tested for Quiescent Current at 20V
- Standardized, Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Full Package-Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"

Applications

- Scratch Pad Memories
- Arithmetic Units
- Data Storage

Description

The CD40208BMS is a 4 x 4 multiport register containing four 4-bit registers, write address decoder, two separate read address decoders, and two 3-state output buses.

When the ENABLE input is low, the corresponding output bus is switched, independently of the clock, to a high impedance state. The high impedance third state provides the outputs with the capability of being connected to the bus lines in a bus organized system without the need for interface or pull-up components.

When the WRITE ENABLE input is high, all data input lines are latched on the positive transition of the CLOCK and the data is entered into the word selected by the write address lines. When WRITE ENABLE is low, the CLOCK is inhibited and no new data is entered. In either case, the contents of any word may be accessed via the read address lines independent of the state of the CLOCK input.

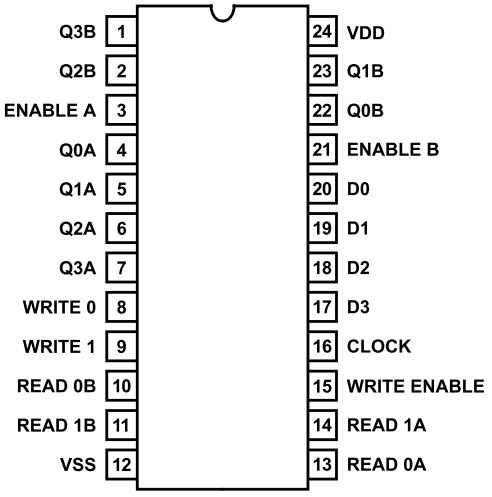
The CD40208BMS types are supplied in hermetic 24-lead dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD40208BMS is supplied in these 24-lead outline packages:

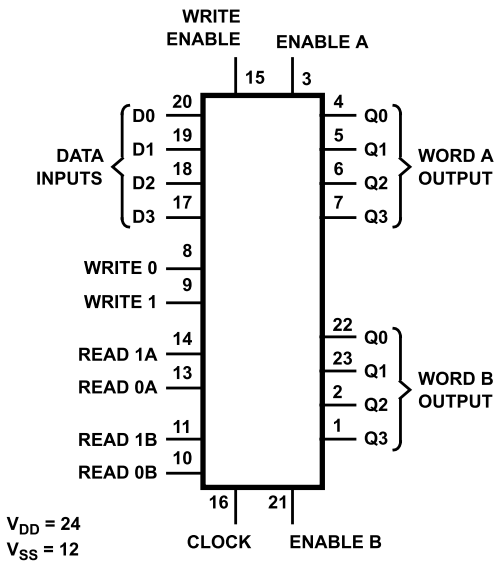
Braze Seal DIP	HNZ
Ceramic Flatpack	H4P

Pinout

CD40208BMS
TOP VIEW



Functional Diagram



Specifications CD40208BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and Frit Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K) 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/NoGo test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock or Write Enable to Q	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	720	ns
			10, 11	+125°C, -55°C	-	972	ns
Propagation Delay Read or Write Enable to Q	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay 3-State Disable Delay Time	TPZH, HZ	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Propagation Delay 3-State Disable Delay Time	TPZL, LZ	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	260	ns
			10, 11	+125°C, -55°C	-	351	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	1.5	-	MHz
			10, 11	+125°C, -55°C	1.11	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL4	VDD = 4.5V, VOUT = 0.4V	1, 2	+125°C	-	-	mA
				-55°C	-	-	mA
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock or Write Enable to Q	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	280	ns
		VDD = 15V	1, 2, 3	+25°C	-	200	ns
Propagation Delay Read or Write Address to Q	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Propagation Delay Output Disable to Output	TPZL, LZ	VDD = 10V	1, 2, 4	+25°C	-	120	ns
		VDD = 15V	1, 2, 4	+25°C	-	100	ns
Propagation Delay Output Disable to Output	TPZH, HZ	VDD = 10V	1, 2, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 4	+25°C	-	80	ns
Minimum Write Enable to $\overline{\text{Clock}}$ Setup Time	TS (WE)	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Minimum Data to Clock Setup Time	TS (D)	VDD = 5V	1, 2, 3	+25°C	-	0	ns
		VDD = 10V	1, 2, 3	+25°C	-	0	ns
		VDD = 15V	1, 2, 3	+25°C	-	0	ns
Minimum Write Address to $\overline{\text{Clock}}$ Setup Time	TS (WA)	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Minimum Write Enable to Clock Hold Time	TH (WE)	VDD = 5V	1, 2, 3	+25°C	-	270	ns
		VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Data to Clock Hold Time	TH (D)	VDD = 5V	1, 2, 3	+25°C	-	220	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Write Address to $\overline{\text{Clock}}$ Hold Time	TH (WA)	VDD = 5V	1, 2, 3	+25°C	-	330	ns
		VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Minimum Clock Pulse Width, Clock or Write Enable	TW (CL)	VDD = 5V	1, 2, 3	+25°C	-	350	ns
		VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Minimum Clock Pulse Width, Write Address	TW (WA)	VDD = 5V	1, 2, 3	+25°C	-	300	ns
		VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	3.5	-	MHz
		VDD = 15V	1, 2, 3	+25°C	4.5	-	MHz
Clock Rise and Fall Time	tRCL tFCL	VDD = 5V	1, 2, 3	+25°C	-	15	µs
		VDD = 10V	1, 2, 3	+25°C	-	5	µs
		VDD = 15V	1, 2, 3	+25°C	-	5	µs
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K., Input TR, TF < 20ns
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS= -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES:

1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input tR, tF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record.

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	1, 2, 4-7, 22, 23	3, 8-21	24			
Static Burn-In 2 (Note 1)	1, 2, 4-7, 22, 23	12	3, 8-11, 13-21, 24			
Dynamic Burn-In (Note 1)		12	3, 15, 16, 21, 24	1, 2, 4-7, 22, 23	8, 10, 14, 19, 20	9, 11, 13, 17, 18
Irradiation (Note 2)	1, 2, 4-7, 22, 23	12	3, 8-11, 13-21, 24			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Block Diagram

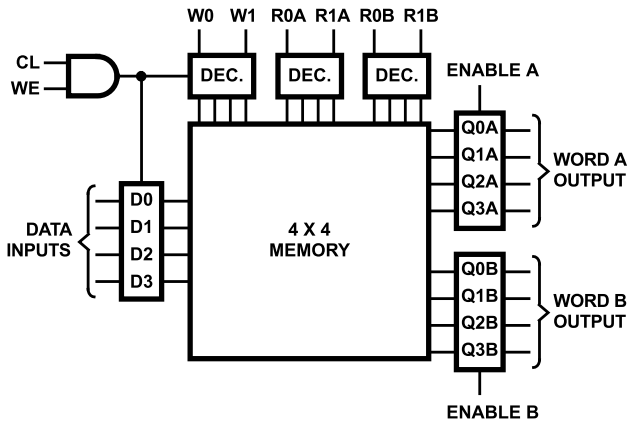


FIGURE 1.

Logic Diagram

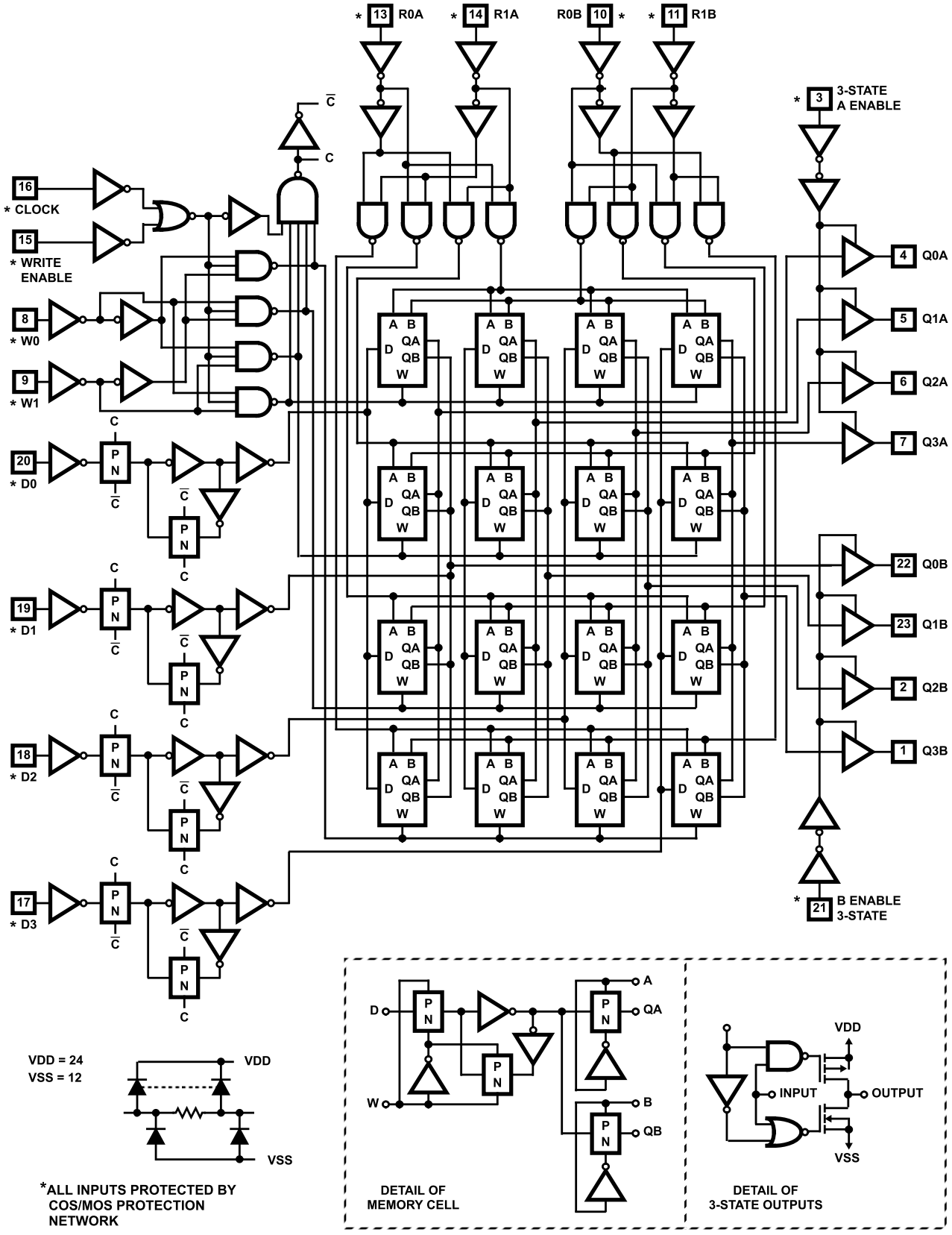


FIGURE 2.

TRUTH TABLE

CLOCK	WRITE ENABLE	WRITE 1	WRITE 0	READ 1A	READ 0A	READ 1B	READ 0B	ENABLE A	ENABLE B	Dn	QnA	QnB
⎍	1	S1	S2	S1	S2	S1	S2	1	1	1	1	1
⎍	1	S1	S2	S1	S2	S1	S2	1	1	0	0	0
X	X	X	X	X	X	X	X	0	0	X	Z	Z
⎍	1	0	0	0	1	1	0	1	1	Dn to Word 0	Word 1 Out	Word 2 Out
⎍	0	0	0	0	1	1	0	1	1	Word 0 Not Altered	Word 1 Out	Word 2 Out
X	X	X	X	1	0	0	1	1	1	X	Word 2 Out	Word 1 Out
⎎	X	X	X	X	X	X	X	1	1	X	NC	NC

1 = High Level; 0 = Low Level; X = Don't Care; Z = High Impedance

NOTE: S1 and S2 refer to input states of either 1 or 0.

Typical Performance Characteristics

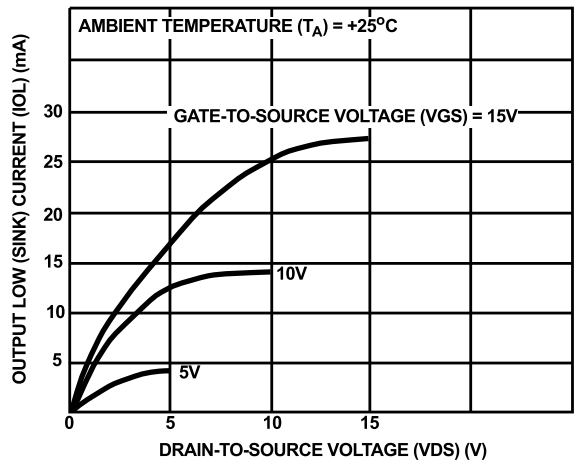


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

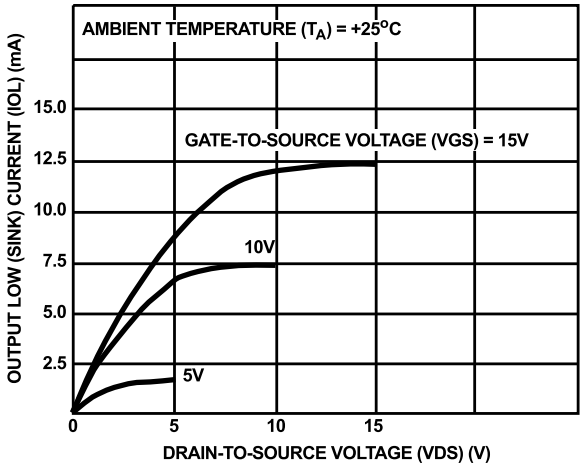


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

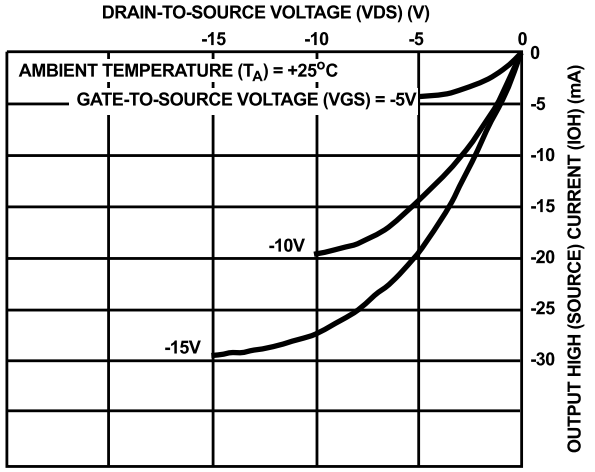


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

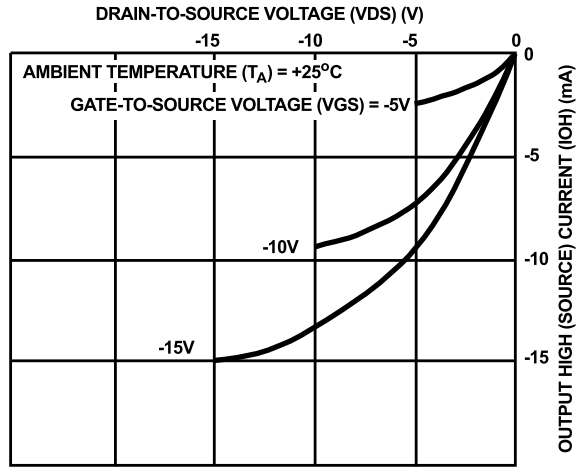


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

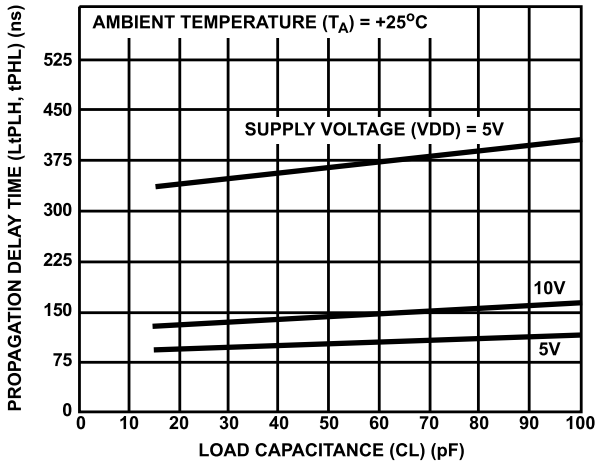


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CL OR WE TO Q)

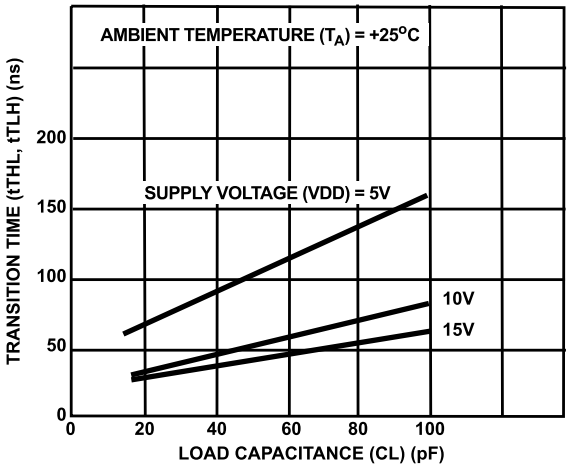


FIGURE 8. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

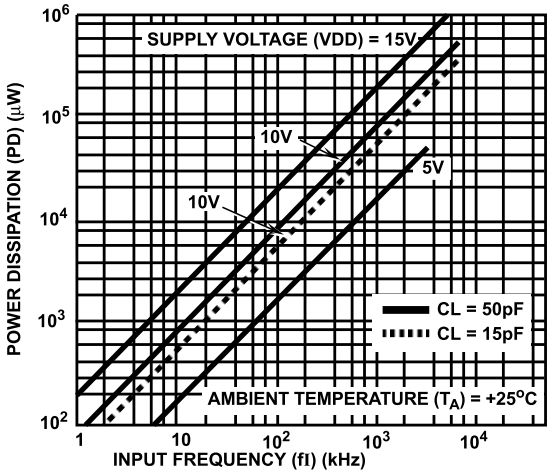


FIGURE 9. TYPICAL POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

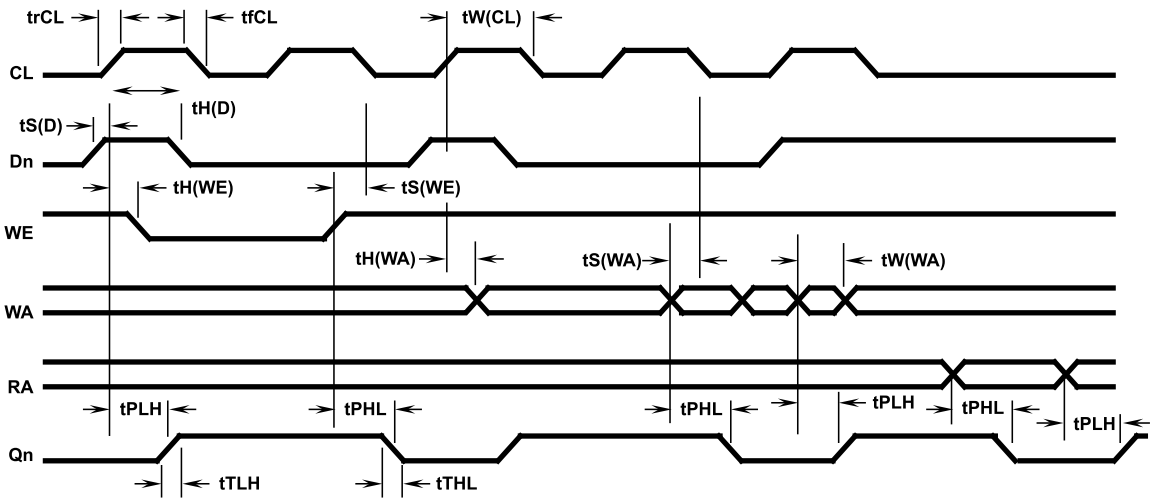


FIGURE 10. TIMING DIAGRAM

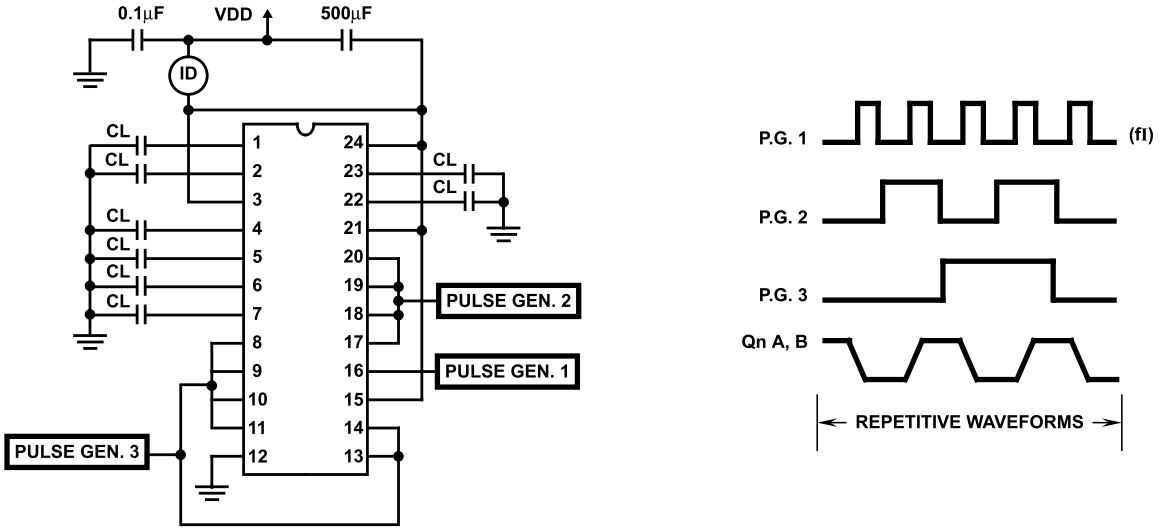
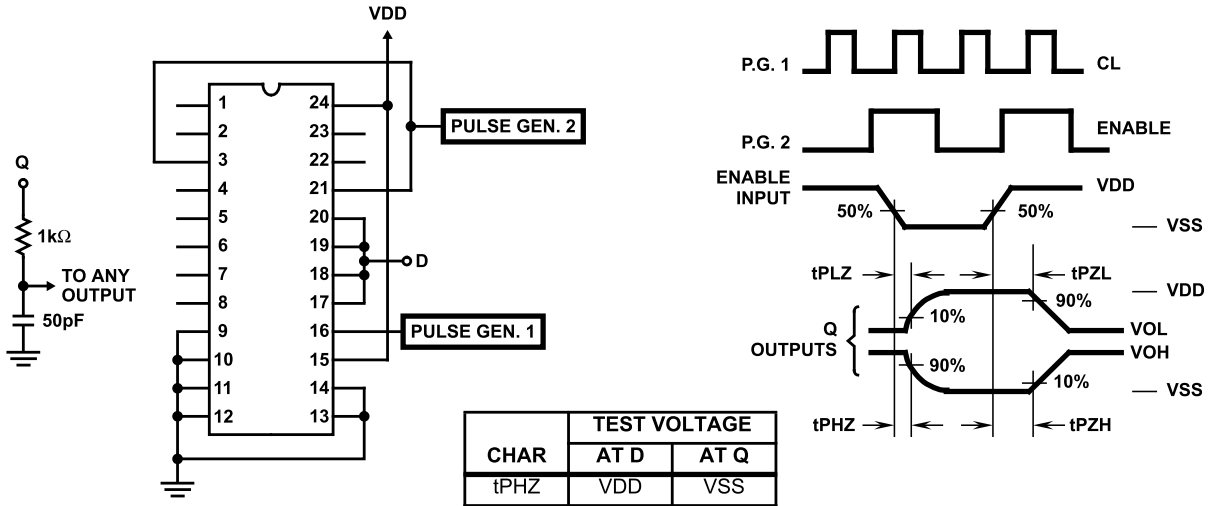


FIGURE 11. POWER-DISSIPATION TEST CIRCUIT AND WAVEFORMS



CHAR	TEST VOLTAGE	
	AT D	AT Q
tPHZ	VDD	VSS
tPZH	VDD	VSS
tPLZ	VSS	VDD
tPZL	VSS	VDD

FIGURE 12. OUTPUT-ENABLE-DELAY-TIMES TEST CIRCUIT AND WAVEFORMS