4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

- MEDIUM-SPEED OPERATION: f_{CL}= 9 MHz (TYP.) @ V_{DD}= 10V
- FULLY STATIC OPERATION
- SYNCHRONOUS PARALLEL OR SERIAL OPERATION
- THREE-STATE OUTPUTS (**HCC/HCF 40104B**)
- ASYNCHRONOUS MASTER RESET (**HCC/HCF 40194B**)
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 40104B, HCC 40194B,** (extended temperature range) and the **HCC 40104B, HCF 40194B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 40104B** is a universal shift register featuring parallel inputs, parallel outputs, SHIFT RIGHT and SHIFT LEFT serial inputs, and a high-impedance third output state allowing the device to be used in bus-organized systems. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clearing the register is accomplished by setting both mode controls low and clocking the register. When the output enable input is low, all outputs assume the high impedance state. The **HCC/HCF 40194B** is a universal shift register featuring parallel inputs, parallel outputs SHIFT RIGHT and SHIFT LEFT serial inputs, and a direct overriding clear input. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right and shift left are accomplished synchronously on the positive clock edge with data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clocking of the register is inhibited when both mode control inputs are low. When low, the $\overline{\text{RESET}}$ input resets all stages and forces all outputs low. The **HCC/HCF 40194B** is similar to industry types 340194 and MC40194.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_i	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

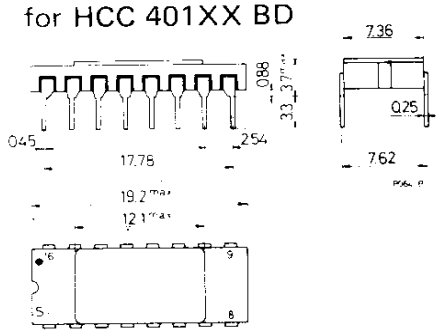
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

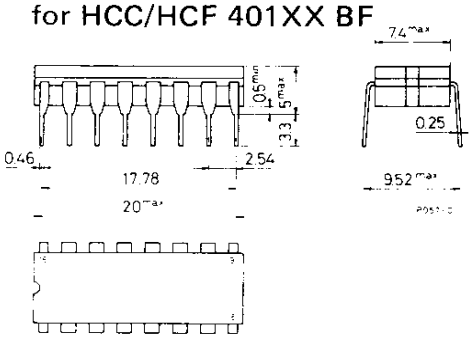
HCC 401XX BD for dual in-line ceramic package
HCC 401XX BF for dual in-line ceramic package, frit seal
HCC 401XX BK for ceramic flat package
HCF 401XX BE for dual in-line plastic package
HCF 401XX BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

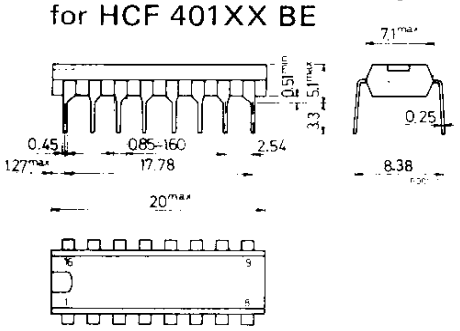
Dual in-line ceramic package
for HCC 401XX BD



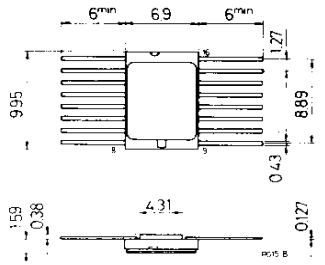
Dual in-line ceramic package
for HCC/HCF 401XX BF



Dual in-line plastic package
for HCF 401XX BE

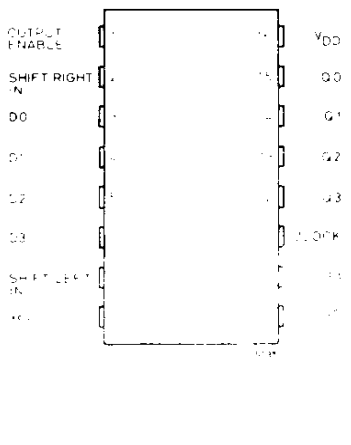


Ceramic flat package
for HCC 401XX BK

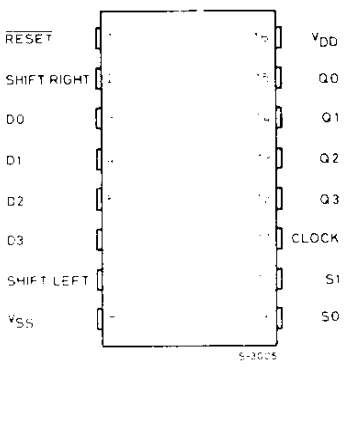


PIN CONNECTIONS

40104

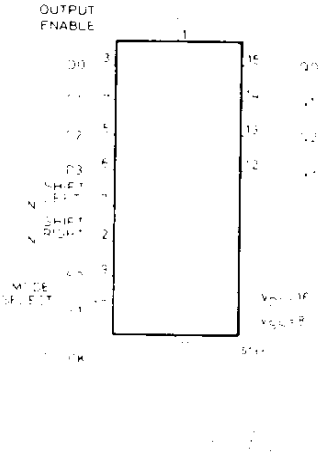


40194

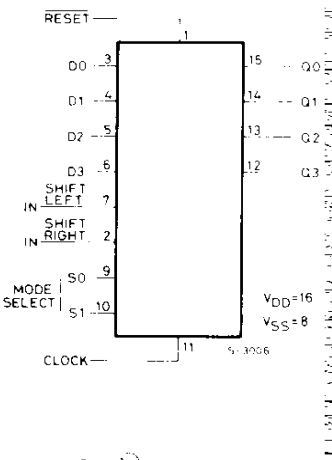


FUNCTIONAL DIAGRAMS

40104



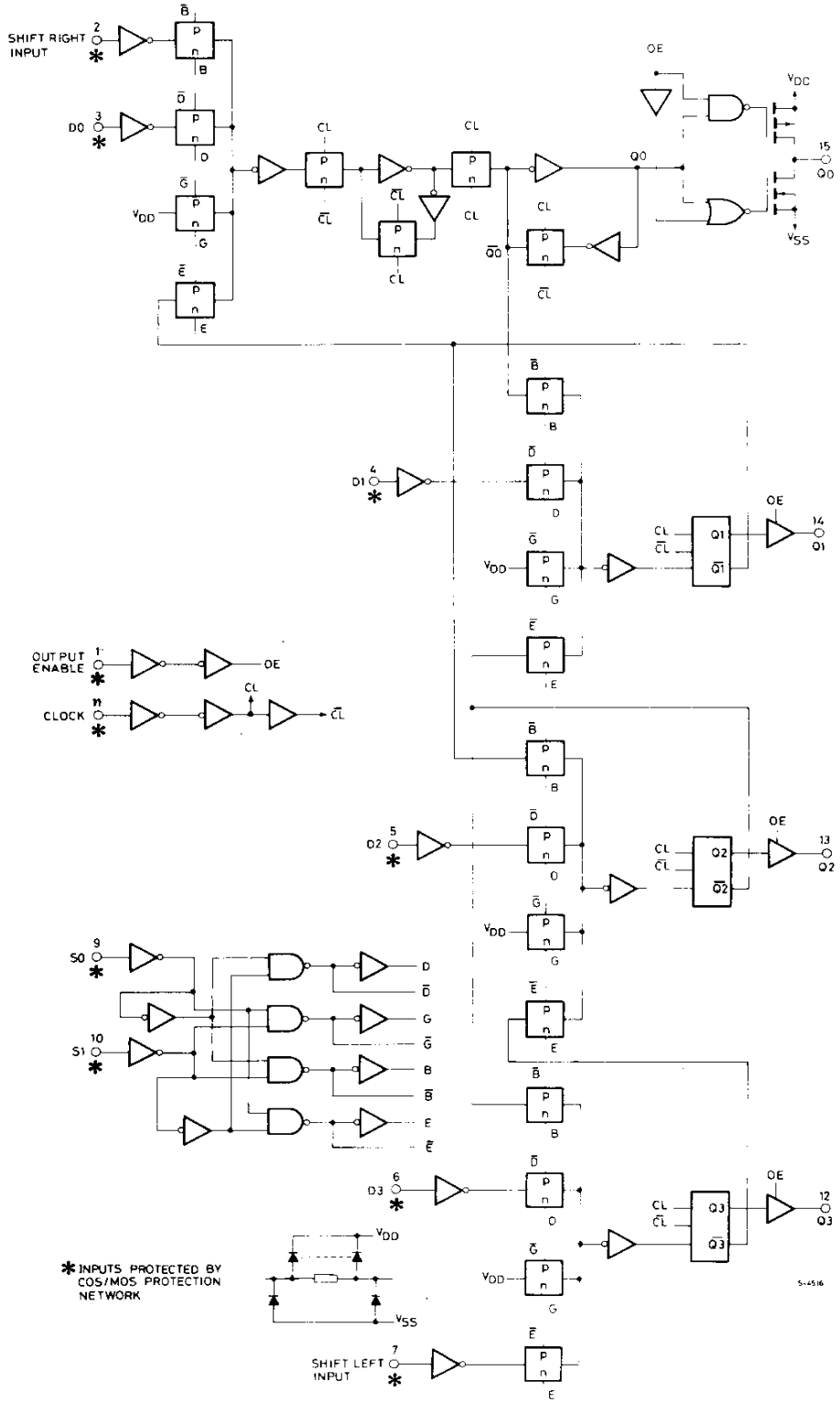
40194



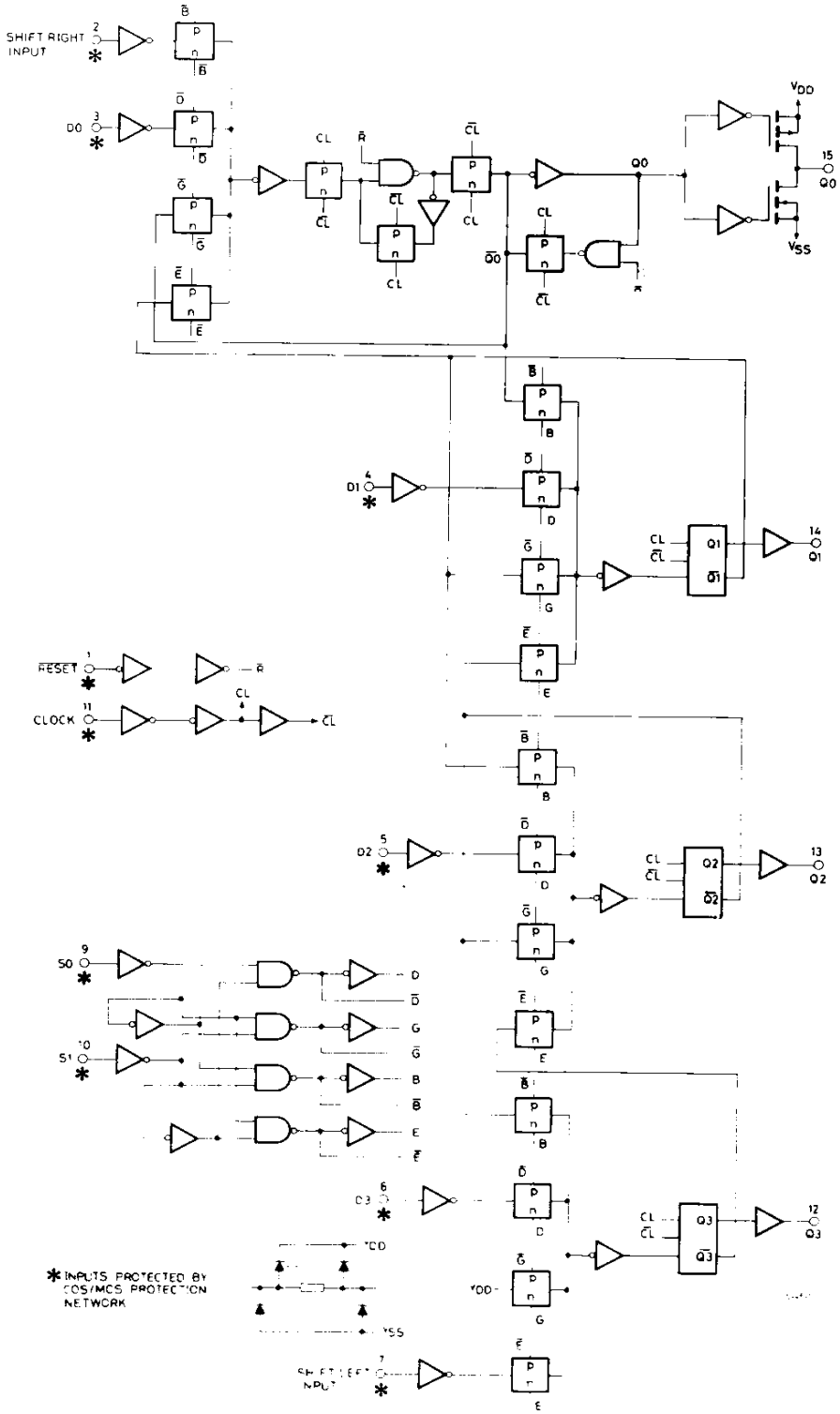
RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

LOGIC DIAGRAM
For 40104B



LOGIC DIAGRAM
For 40194B



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
		HCF types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		± 1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = − 55°C for **HCC** device: −40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time Clock to Q	5		220	440	ns
		10		100	200	
		15		70	140	
t_{PZH}, t_{PZL}	3-state outputs ■	5		80	160	ns
t_{PLZ}	High Impedance	10		35	70	
		15		25	50	
t_{PHZ}		5		45	90	ns
		10		25	50	
		15		20	40	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
t_{setup}	Setup time D0, D3, SR, SL to Clock	5		80	100	ns
		10		35	70	
		15		20	50	
	S0, S1 to Clock	5		200	400	ns
		10		110	220	
		15		65	130	
t_{hold}	Hold time D0, D3, SR, SL to Clock	5		-65	0	ns
		10		-25	0	
		15		-15	0	
	S0, S1 to Clock	5		-170	0	ns
		10		-95	0	
		15		-55	0	
t_W	Clock pulse width	5		90	180	ns
		10		40	180	
		15		25	50	
f_{CL}	Clock input frequency	5	3	6		MHz
		10	6	12		
		15	8	15		
t_r, t_f	Clock input rise or fall time	5			1000	μs
		10			100	
		15			100	
t_W	Reset pulse width *	5		150	300	ns
		10		100	200	
		15		70	140	
t_{PRHL}	Propagation Delay Reset *	5		230	460	ns
		10		90	180	
		15		65	130	

■ For 40104B series only * For 40194B series only.

TRUTH TABLES

For **40104B**

CLOCK▲	MODE SELECT		OUTPUT ENABLE	ACTION
	S0	S1		
⌐¯	0	0	1	Reset
⌐¯	1	0	1	Shift right (Q0 toward Q3)
⌐¯	0	1	1	Shift left (Q3 toward Q0)
⌐¯	1	1	1	Parallel load
X	X	X	0	Operations occur as shown above, but outputs assume high impedance

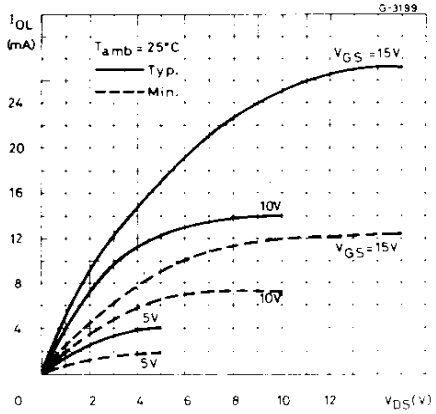
For **40194B**

CLOCK	MODE SELECT		$\overline{\text{RESET}}$	ACTION
	S0	S1		
X	0	0	1	No Change
⌐¯	1	0	1	Shift Right (Q0 toward Q3)
⌐¯	0	1	1	Shift Left (Q3 toward Q0)
⌐¯	1	1	1	Parallel Load
X	X	X	0	Reset

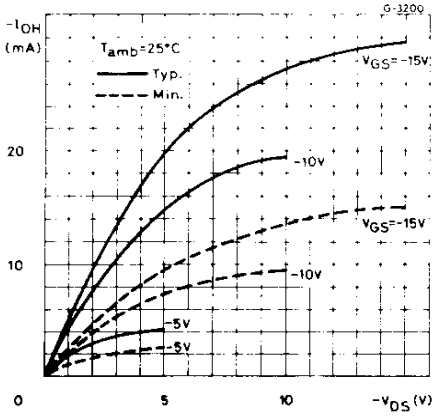
1 = High level
0 = Low level

X = Don't care
▲ = Level change

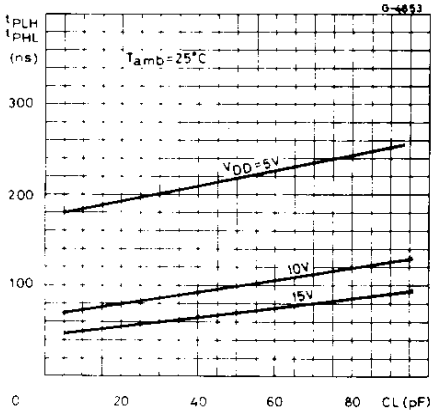
Output low (sink) current characteristics



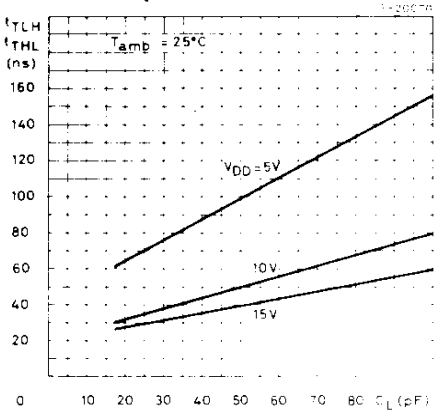
Output high (source) current characteristics



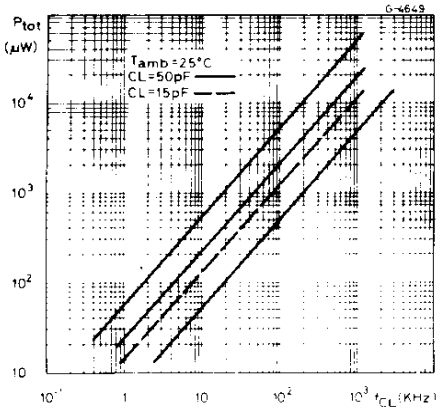
Typical propagation delay time vs. load capacitance



Typical transition time vs. load capacitance

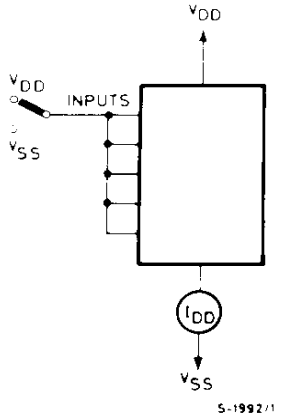


Typical dynamic power dissipation vs. frequency

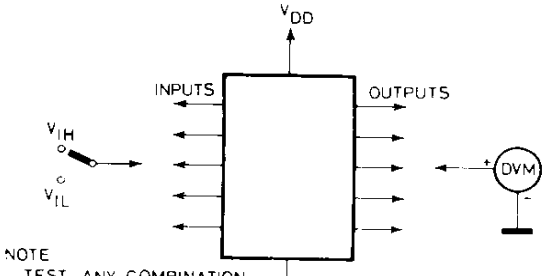


TEST CIRCUITS

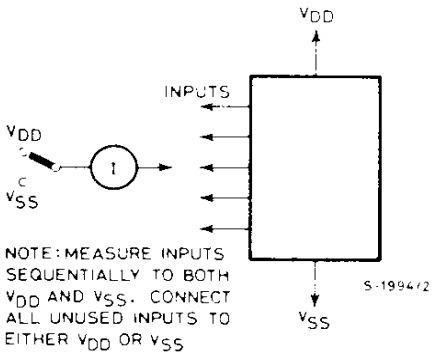
Quiescent device current



Input voltage



Input leakage current



Dynamic power dissipation