

Quadruple static decade counters

HEF4737B
HEF4737V

DESCRIPTION

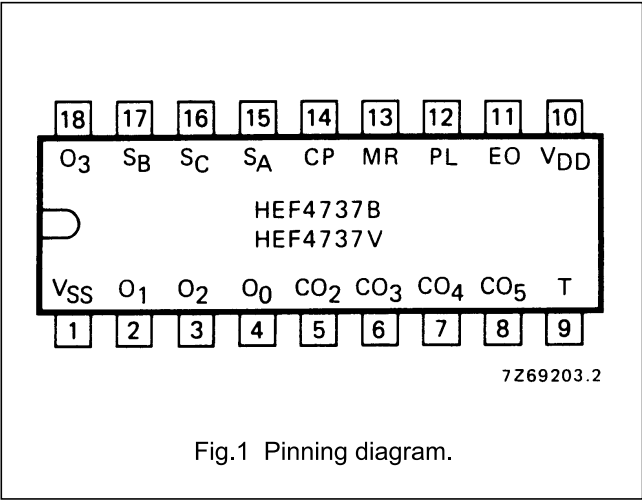
The HEF4737B and HEF4737V are static quadruple decade counters for frequencies from 0 to 10 MHz. The counters are supplied with an extra overload flip-flop giving a total count capability of 19 999. The counter has the following inputs and outputs: a count input (CP), an asynchronous reset input (MR), an asynchronous preset input (PL), a transfer input (T), an output enable input (EO) (which controls the BCD outputs), the digit select inputs (S_A , S_B , S_C) (which perform selection of the contents of the latches to the 3-state BCD outputs (O_0 to O_3)), and the carry outputs (CO_2 to CO_5) (which give the carry signals of the decades except from the first decade).

The complementary MOS structure gives the devices very low stand-by and operating dissipation. Operating from a single supply voltage all outputs can drive one standard TTL input without interface circuitry under all specified operating conditions.

The BCD digit outputs are LOCMOS 3-state outputs. The high impedance off-state feature allows common busing of the outputs. The counters are supplied with asynchronous reset and preset to 19 999 facilities making them suitable for counter and time base applications. All carry signals are available except from the first decade.

Schmitt-trigger action in the inputs makes the circuit highly tolerant to slower input rise and fall times.

Recommended supply voltage range for HEF4737B is 3 to 15 V and for HEF4737V is 4,5 to 12,5 V.



PINNING

- CP
- count input
- MR
- asynchronous reset input
- PL
- asynchronous preset input
- T
- transfer input
- S_A , S_B , S_C
- digit select inputs
- EO
- output enable input
- O_0 to O_3
- BCD outputs
- CO_2 to CO_5
- carry outputs

HEF4737BP; HEF4737VP(N); 18-lead DIL plastic (SOT102-1)

HEF4737BD; HEF4737VD(F); 18-lead DIL ceramic (SOT133B)

(): Package Designator North America

SUPPLY VOLTAGE

	RATING	RECOMMENDED OPERATING	
HEF4737B	−0,5 to 18	3,0 to 15,0	V
HEF4737V	−0,5 to 18	4,5 to 12,5	V

FAMILY DATA, I_{DD} LIMITS category LSI

See Family Specifications

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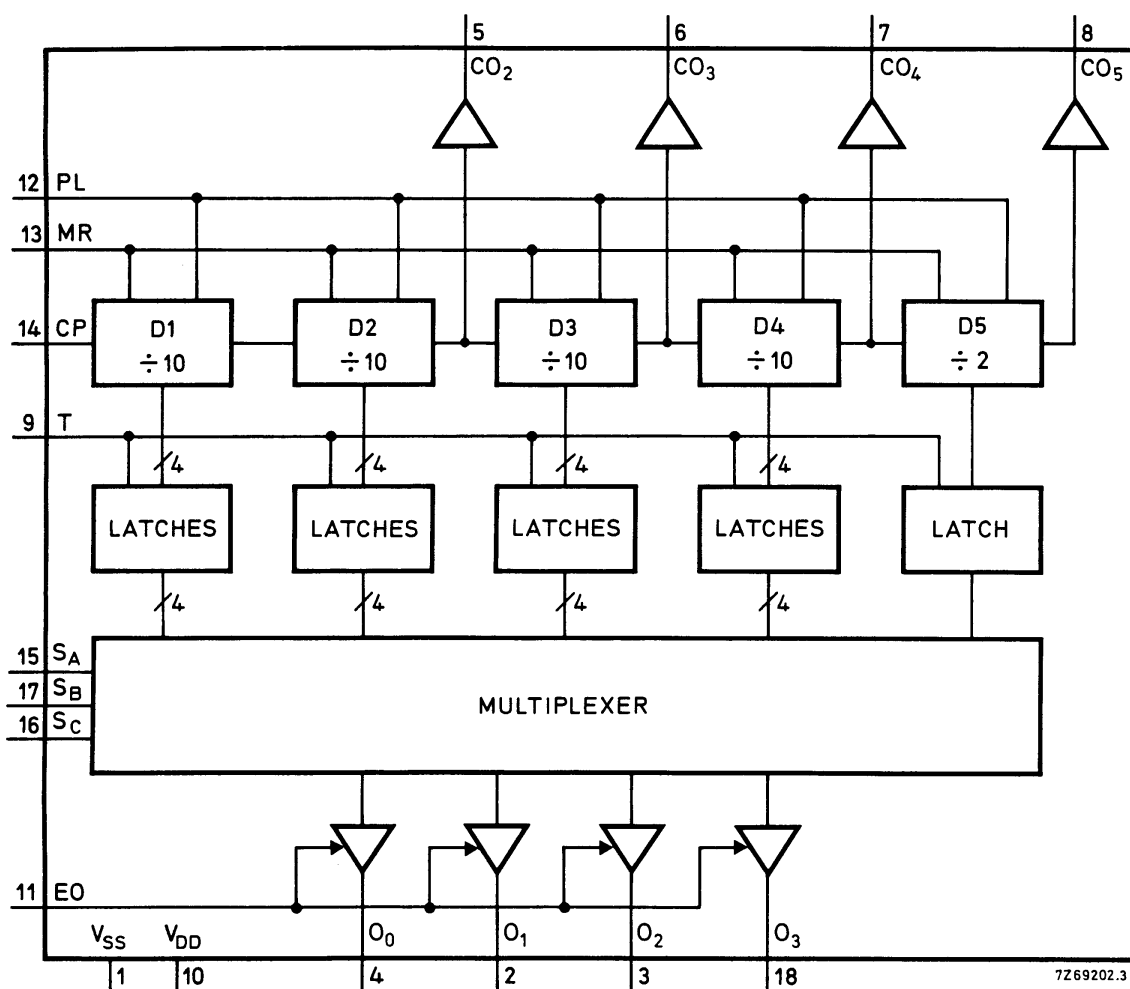


Fig.2 Block diagram.

FUNCTIONAL DESCRIPTION

Input signals

Count input (CP)

The signal to be counted is applied to this input. When PL and MR are LOW the contents of the counter increments by one at a LOW to HIGH transition of CP.

Reset input (MR)

This is an asynchronous reset. A HIGH level applied to this input will reset the counter to zero independent of the level at the count input and preset input.

Preset input (PL)

This is an asynchronous preset. When MR is LOW a HIGH at the PL input will preset the counter to 19 999 independent of the level at the count input.

Transfer input (T)

A HIGH level applied to this input allows the information held by the counter to pass to the latches.

Output enable input (EO)

A HIGH level at this input enables the BCD outputs and information can be read out of the latches using the

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multiplexer. A LOW level at this input disables the BCD outputs making them floating (high impedance off-state).

Digit select inputs (S_A , S_B , S_C)

S_A	S_B	S_C	
L	L	L	selects D1 (LSD)
H	L	L	selects D2
L	H	L	selects D3
H	H	L	selects D4
X	X	H	selects D5 (MSD)

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial
4. When D5 is selected, the contents of D5 is available at O_0 and O_1 , O_2 and O_3 are LOW.
5. LSD = least significant divider
6. MSD = most significant divider

Output signals

The carry outputs are active LOW outputs.

Carry output CO_2

When the contents of the first two decades of the counter are both 9 then the CO_2 output becomes LOW. It remains LOW until the next LOW to HIGH transition of the count input, i.e. until the contents of the first two decades are zero. CO_2 is LOW when the contents of the counter are: 00 099, 00 199, 00 299 etc.

Carry output CO_3

When the contents of the first three decades of the counter are all 9 then the CO_3 output becomes LOW. It remains LOW until the next LOW to HIGH transition of the count input, i.e. until the contents of the first three decades are zero. CO_3 is LOW when the contents of the counter are 00 999, 01 999, 02 999 etc.

Carry output CO_4

When the contents of the first four decades of the counter are all 9 then the CO_4 output becomes LOW. It remains LOW until the next LOW to HIGH transition of the count input, i.e. until the contents of the first four decades are zero. CO_4 is LOW when the contents of the counter are 09 999 and 19 999.

The carry signals CO_2 , CO_3 and CO_4 are suppressed while the preset is active. A HIGH to the preset input sets the counter to 19 999 but the carry signals remain HIGH until preset input returns to LOW, then the carry outputs will also become LOW.

Carry output CO_5

When the content of the counter is 10 000 the CO_5 output becomes LOW. It returns to HIGH when the content of the counter is zero.

Digit outputs (O_0 to O_3)

The digit outputs give the contents of the selected latch. The output is in the form of BCD, positive logic.

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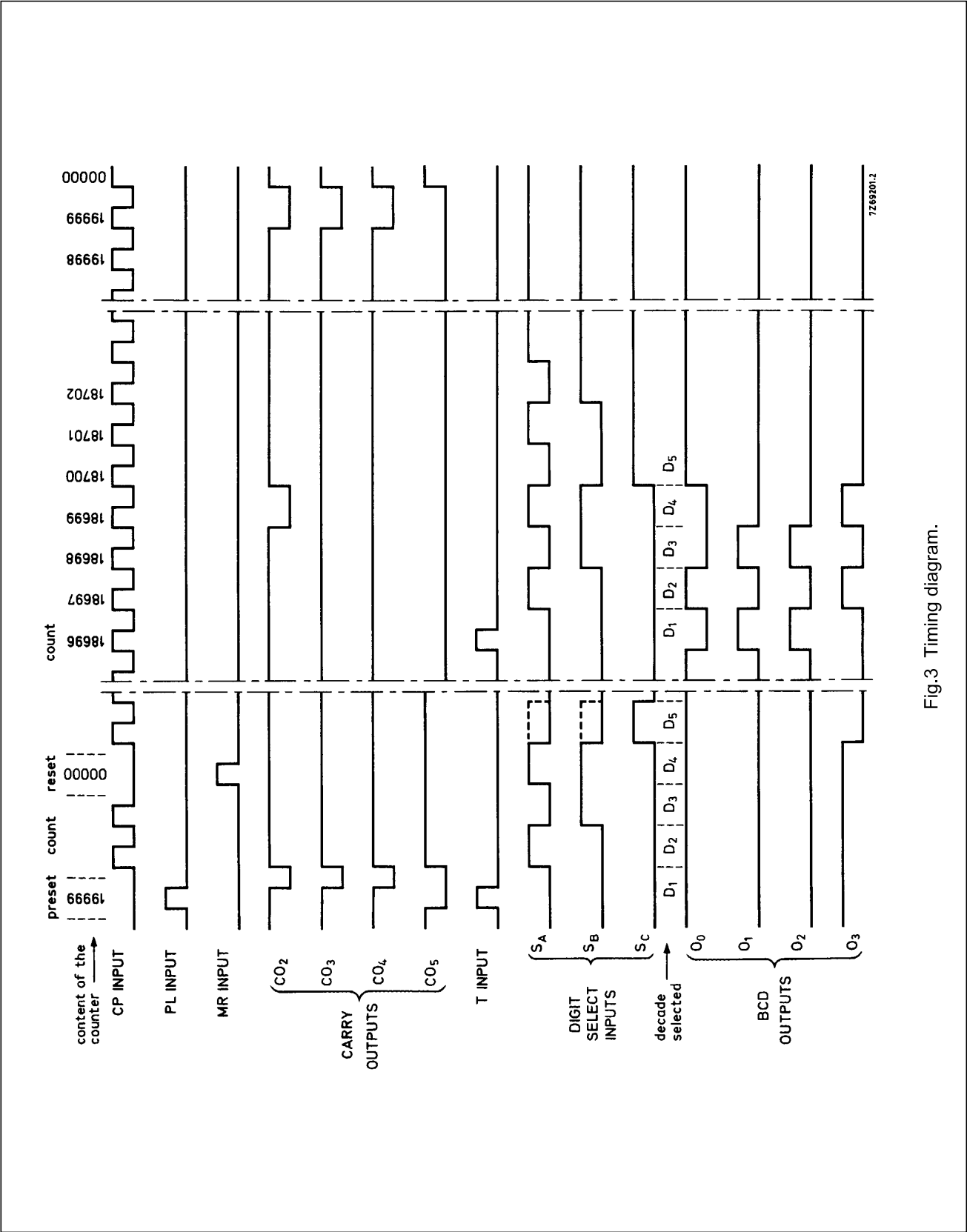


Fig.3 Timing diagram.

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The values given at $V_{DD} = 15\text{ V}$ in the following d.c. and a.c. characteristics, are not applicable to the HEF4737V, because of its reduced supply voltage range.

DC CHARACTERISTICS

$V_{SS} = 0\text{ V}$

	V_{DD} V	V_{OH} V	V_{OL} V	SYMBOL	$T_{amb} (^{\circ}\text{C})$					
					-40		+ 25		+ 85	
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Input leakage current at $V_I = 0$ or V_{DD}	10			$\pm I_{IN}$	–	–	–	0,3	–	1 μA
	15				–	–	–	0,3	–	1 μA
Output (sink) current LOW	4,75		0,4	I_{OL}	1,6	–	1,6	–	1,4	– mA
	10		0,5		2,5	–	2,3	–	1,7	– mA
	15		1,5		7,0	–	6,0	–	4,0	– mA
Output (source) current HIGH	5	4,6		$-I_{OH}$	0,96	–	0,80	–	0,65	– mA
	10	9,5			2,4	–	2,0	–	1,6	– mA
	15	13,5			7,0	–	6,0	–	4,5	– mA
Output (source) current HIGH	5	2,5		$-I_{OH}$	3,0	–	2,5	–	2,0	– mA
3-state output leakage current $V_O = 0$ or V_{DD}	10			$\pm I_{OZ}$	–	1,6	–	1,6	–	12 μA
	15				–	1,6	–	1,6	–	12 μA

AC CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25^{\circ}\text{C}$; $C_L = 15\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays CP $\rightarrow$ O _n (D1 selected) HIGH to LOW LOW to HIGH	5	t_{PHL}		320	640 ns	308 ns + (0,24 ns/pF) C_L
	10			120	240 ns	125 ns + (0,10 ns/pF) C_L
	15			90	180 ns	86 ns + (0,07 ns/pF) C_L
	5	t_{PLH}		320	640 ns	296 ns + (0,48 ns/pF) C_L
	10			120	240 ns	110 ns + (0,20 ns/pF) C_L
	15			90	180 ns	82 ns + (0,15 ns/pF) C_L
CP $\rightarrow$ O _n (D5 selected) HIGH to LOW LOW to HIGH	5	t_{PHL}		620	1240 ns	608 ns + (0,24 ns/pF) C_L
	10			330	660 ns	325 ns + (0,10 ns/pF) C_L
	15			250	500 ns	246 ns + (0,07 ns/pF) C_L
	5	t_{PLH}		620	1240 ns	596 ns + (0,48 ns/pF) C_L
	10			330	660 ns	320 ns + (0,20 ns/pF) C_L
	15			250	500 ns	242 ns + (0,15 ns/pF) C_L

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	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
CP → CO ₂	5			220	440	ns	208 ns + (0,24 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		110	220	ns	105 ns + (0,10 ns/pF) C _L
	15			85	170	ns	81 ns + (0,07 ns/pF) C _L
	5	t _{PLH}		220	400	ns	196 ns + (0,48 ns/pF) C _L
	10			110	220	ns	100 ns + (0,20 ns/pF) C _L
	15			85	170	ns	77 ns + (0,15 ns/pF) C _L
Propagation delays							
CP → CO ₅	5			350	700	ns	338 ns + (0,24 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		160	320	ns	155 ns + (0,10 ns/pF) C _L
	15			120	240	ns	116 ns + (0,07 ns/pF) C _L
	5		t _{PLH}		350	700	ns
10		160		320	ns	150 ns + (0,20 ns/pF) C _L	
15		120		240	ns	112 ns + (0,15 ns/pF) C _L	
LOW to HIGH							
S _n → O _n	5			200	400	ns	188 ns + (0,24 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		80	160	ns	75 ns + (0,10 ns/pF) C _L
	15			55	110	ns	51 ns + (0,07 ns/pF) C _L
	5		t _{PLH}		200	400	ns
10		80		160	ns	70 ns + (0,20 ns/pF) C _L	
15		55		110	ns	47 ns + (0,15 ns/pF) C _L	
LOW to HIGH							
T→ O _n	5			220	440	ns	208 ns + (0,24 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		90	180	ns	85 ns + (0,10 ns/pF) C _L
	15			60	120	ns	56 ns + (0,07 ns/pF) C _L
	5		t _{PLH}		220	440	ns
10		90		180	ns	80 ns + (0,20 ns/pF) C _L	
15		60		120	ns	52 ns + (0,15 ns/pF) C _L	
LOW to HIGH							
MR → O _n	5			490	980	ns	478 ns + (0,24 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		200	400	ns	195 ns + (0,10 ns/pF) C _L
	15			60	120	ns	56 ns + (0,07 ns/pF) C _L
	5		t _{PLH}		260	520	ns
10		110		220	ns	100 ns + (0,20 ns/pF) C _L	
15		85		170	ns	77 ns + (0,15 ns/pF) C _L	
LOW to HIGH							
MR → CO _n	5			350	700	ns	326 ns + (0,48 ns/pF) C _L
LOW to HIGH	10	t _{PLH}		160	320	ns	150 ns + (0,20 ns/pF) C _L
	15			120	240	ns	112 ns + (0,15 ns/pF) C _L
	5		t _{PHL}		350	700	ns
10		160		320	ns	155 ns + (0,10 ns/pF) C _L	
15		120		240	ns	116 ns + (0,07 ns/pF) C _L	
PL → CO _n							
HIGH to LOW	5	t _{PHL}		350	700	ns	338 ns + (0,24 ns/pF) C _L
	10			160	320	ns	155 ns + (0,10 ns/pF) C _L
	15			120	240	ns	116 ns + (0,07 ns/pF) C _L

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	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Output transition times; any output HIGH to LOW LOW to HIGH	5	t _{THL}		35	70	ns	15 ns + (0,40 ns/pF) C _L
	10			18	36	ns	9 ns + (0,18 ns/pF) C _L
	15			15	30	ns	8 ns + (0,13 ns/pF) C _L
	5	t _{TLH}		50	100	ns	15 ns + (0,70 ns/pF) C _L
	10			30	60	ns	13 ns + (0,33 ns/pF) C _L
	15			25	50	ns	13 ns + (0,23 ns/pF) C _L
3-state propagation delays							
Output disable times EO → O _n HIGH LOW	5	t _{PHZ}		60	120	ns	
	10			35	70	ns	
	15			25	50	ns	
	5	t _{PLZ}		60	120	ns	
	10			35	70	ns	
	15			25	50	ns	
Output enable times EO → O _n HIGH LOW	5	t _{PZH}		90	180	ns	
	10			40	80	ns	
	15			30	60	ns	
	5	t _{PZL}		90	180	ns	
	10			40	80	ns	
	15			30	60	ns	
Maximum CP pulse width; LOW	5	t _{WCPL}	160	80		ns	
	10		60	30		ns	
	15		50	25		ns	
Minimum MR pulse width; HIGH	5	t _{WMRH}	100	50		ns	
	10		50	25		ns	
	15		40	20		ns	
Minimum PL pulse width; HIGH	5	t _{WPLH}	120	60		ns	
	10		60	30		ns	
	15		50	25		ns	
Minimum T pulse width; HIGH	5	t _{WTH}	100	50		ns	
	10		40	20		ns	
	15		36	18		ns	
Maximum clock pulse frequency	5	f _{max}	3	6		MHz	
	10		8	16		MHz	
	15		10	20		MHz	

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	V_{DD} V	TYPICAL FORMULA FOR P (μ W)	
Dynamic power dissipation per package (P)	5 10 15	$950 f_i + \sum (f_o C_L) \times V_{DD}^2$ $4\ 200 f_i + \sum (f_o C_L) \times V_{DD}^2$ $11\ 200 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)