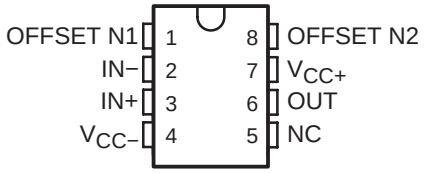
- **Low Noise**
- **No External Components Required**
- **Replace Chopper Amplifiers at a Lower Cost**
- **Wide Input-Voltage Range . . . 0 to ±14 V Typ**
- **Wide Supply-Voltage Range . . . ±3 V to ±18 V**

D OR P PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

These devices offer low offset and long-term stability by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input-voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range. The OP07 is unsurpassed for low-noise, high-accuracy amplification of very-low-level signals.

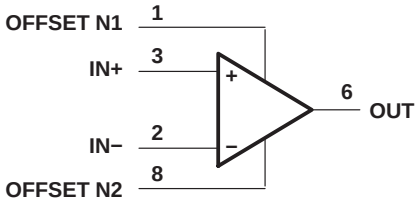
These devices are characterized for operation from 0°C to 70°C.

ORDERING INFORMATION

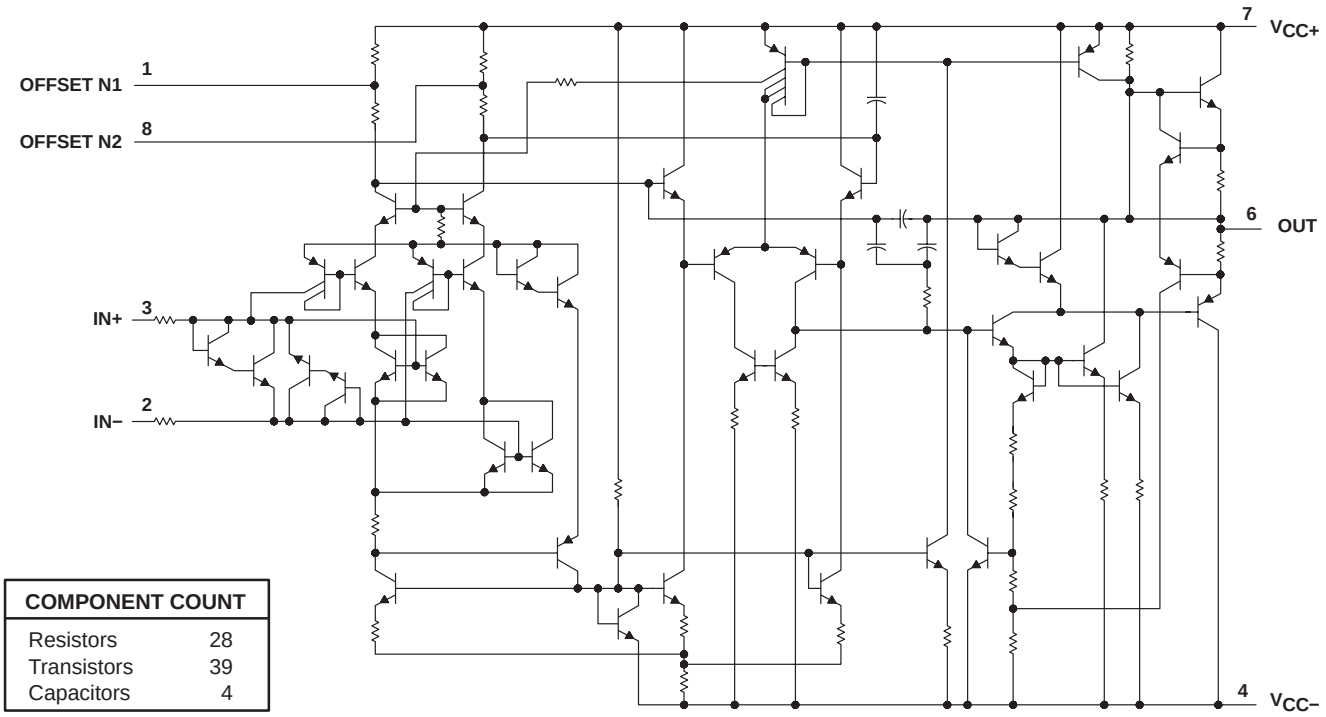
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 50	OP07CP	OP07CP
		Tube of 50	OP07DP	OP07DP
	SOIC (D)	Tube of 75	OP07CD	OP07C
		Reel of 2500	OP07CDR	
		Tube of 75	OP07DD	OP07D
		Reel of 2500	OP07DDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

symbol



schematic



COMPONENT COUNT	
Resistors	28
Transistors	39
Capacitors	4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{CC+} (see Note 1) . . . . . 22 V
V_{CC-} (see Note 1) . . . . . −22 V
Differential input voltage (see Note 2) . . . . . ±30 V
Input voltage, V_I (either input, see Note 3) . . . . . ±22 V
Duration of output short circuit (see Note 4) . . . . . Unlimited
Package thermal impedance, θ_{JA} (see Notes 5 and 6): D package . . . . . 97°C/W
P package . . . . . 85°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either power supply.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage		±3	±18	V
V_{IC}	Common-mode input voltage	$V_{CC\pm}$ = ±15 V	−13	13	V
T_A	Operating free-air temperature		0	70	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	OP07C			OP07D			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0,	R_S = 50 Ω	25°C		60	150		60	150	µV
				0°C to 70°C		85	250		85	250	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0,	R_S = 50 Ω	0°C to 70°C		0.5	1.8		0.7	2.5	µV/°C
	Long-term drift of input offset voltage	See Note 6				0.4			0.5		µV/mo
	Offset adjustment range	R_S = 20 kΩ,	See Figure 1	25°C		±4			±4		mV
I_{IO}	Input offset current			25°C		0.8	6		0.8	6	nA
				0°C to 70°C		1.6	8		1.6	8	
α_{IIO}	Temperature coefficient of input offset current			0°C to 70°C		12	50		12	50	pA/°C
I_{IB}	Input bias current			25°C		±1.8	±7		±2	±12	nA
				0°C to 70°C		±2.2	±9		±3	±14	
α_{IIB}	Temperature coefficient of input bias current			0°C to 70°C		18	50		18	50	pA/°C
V_{ICR}	Common-mode input voltge range			25°C	±13	±14		±13	±14		V
				0°C to 70°C	±13	±13.5		±13	±13.5		
V_{OM}	Peak output voltage	R_L ≥ 10 kΩ		25°C	±12	±13		±12	±13		V
		R_L ≥ 2 kΩ			±11.5	±12.8		±11.5	±12.8		
		R_L ≥ 1 kΩ				±12			±12		
		R_L ≥ 2 kΩ		0°C to 70°C	±11	±12.6		±11	±12.6		
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±3 V, R_L ≥ 500 kΩ	V_O = ±0.5 V,	25°C	100	400			400		V/mV
		V_O = ±10 V,	R_L = 2 kΩ	25°C	120	400		120	400		
				0°C to 70°C	100	400		100	400		
B_1	Unity-gain bandwidth			25°C	0.4	0.6		0.4	0.6		MHz
r_i	Input resistance			25°C	8	33		7	31		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = ±13 V,	R_S = 50 Ω	25°C	100	120		94	110		dB
				0°C to 70°C	97	120		94	106		
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm}$ = ±3 V to ±18 V, R_S = 50 Ω		25°C		7	32		7	32	µV/V
				0°C to 70°C		10	51		10	51	
P_D	Power dissipation	V_O = 0,	No load	25°C		80	150		80	150	mW
		$V_{CC\pm}$ = ±3 V,	V_O = 0, No load			4	8		4	8	

† All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise noted.

NOTE 7: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first 30 days of operation.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS†	OP07C TYP	OP07D TYP	UNIT
V_n	Equivalent input noise voltage	f = 10 Hz	10.5	10.5	nV/√Hz
		f = 100 Hz	10.2	10.3	
		f = 1 kHz	9.8	9.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	0.38	0.38	μV
I_n	Equivalent input noise current	f = 10 Hz	0.35	0.35	pA/√Hz
		f = 100 Hz	0.15	0.15	
		f = 1 kHz	0.13	0.13	
$I_{N(PP)}$	Peak-to-peak equivalent input noise current	f = 0.1 Hz to 10 Hz	15	15	pA
SR	Slew rate	$R_L \geq 2$ kΩ	0.3	0.3	V/μs

† All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise noted.

APPLICATION INFORMATION

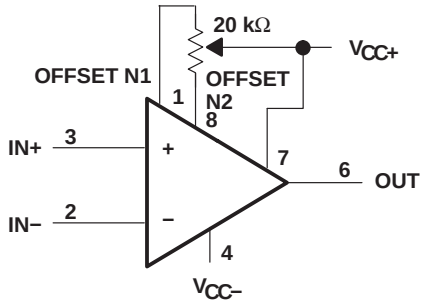
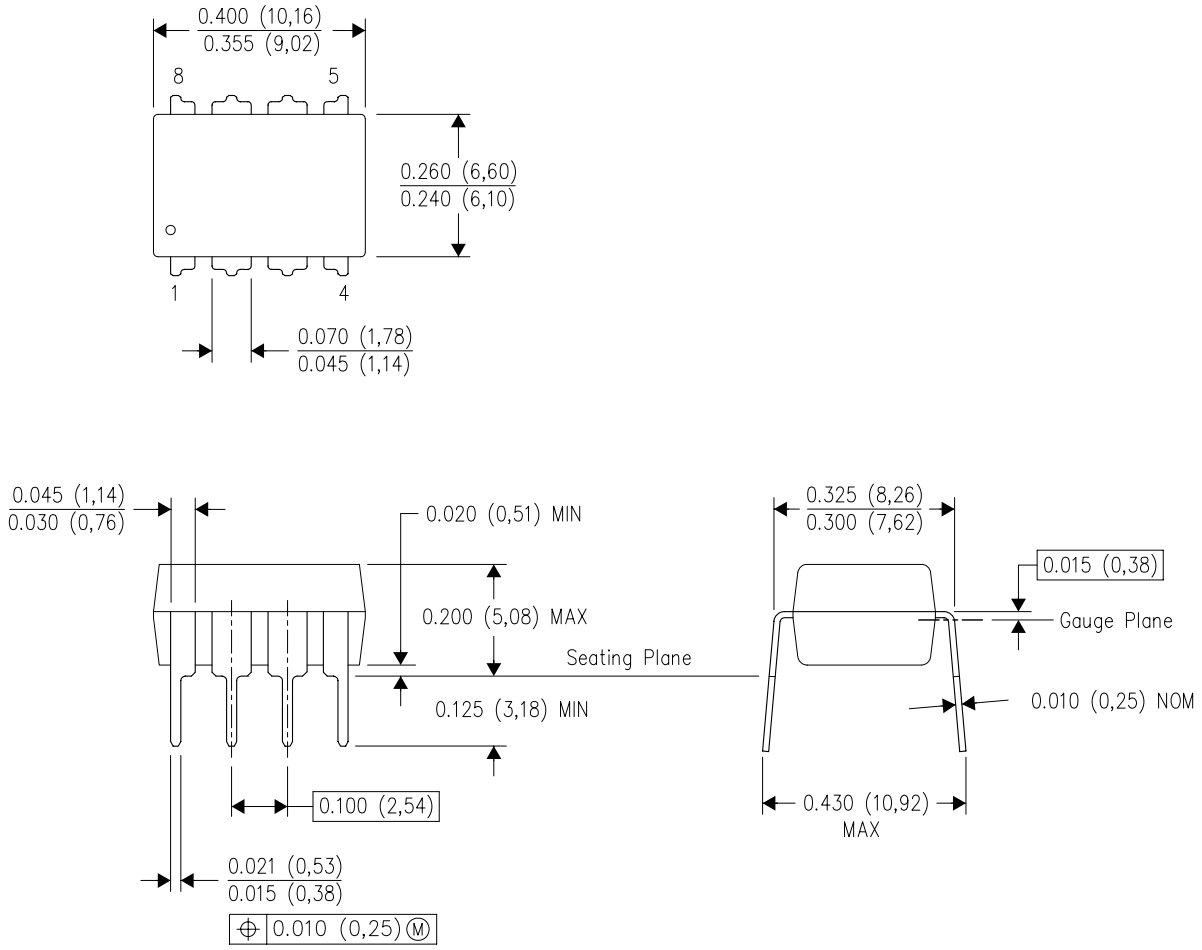


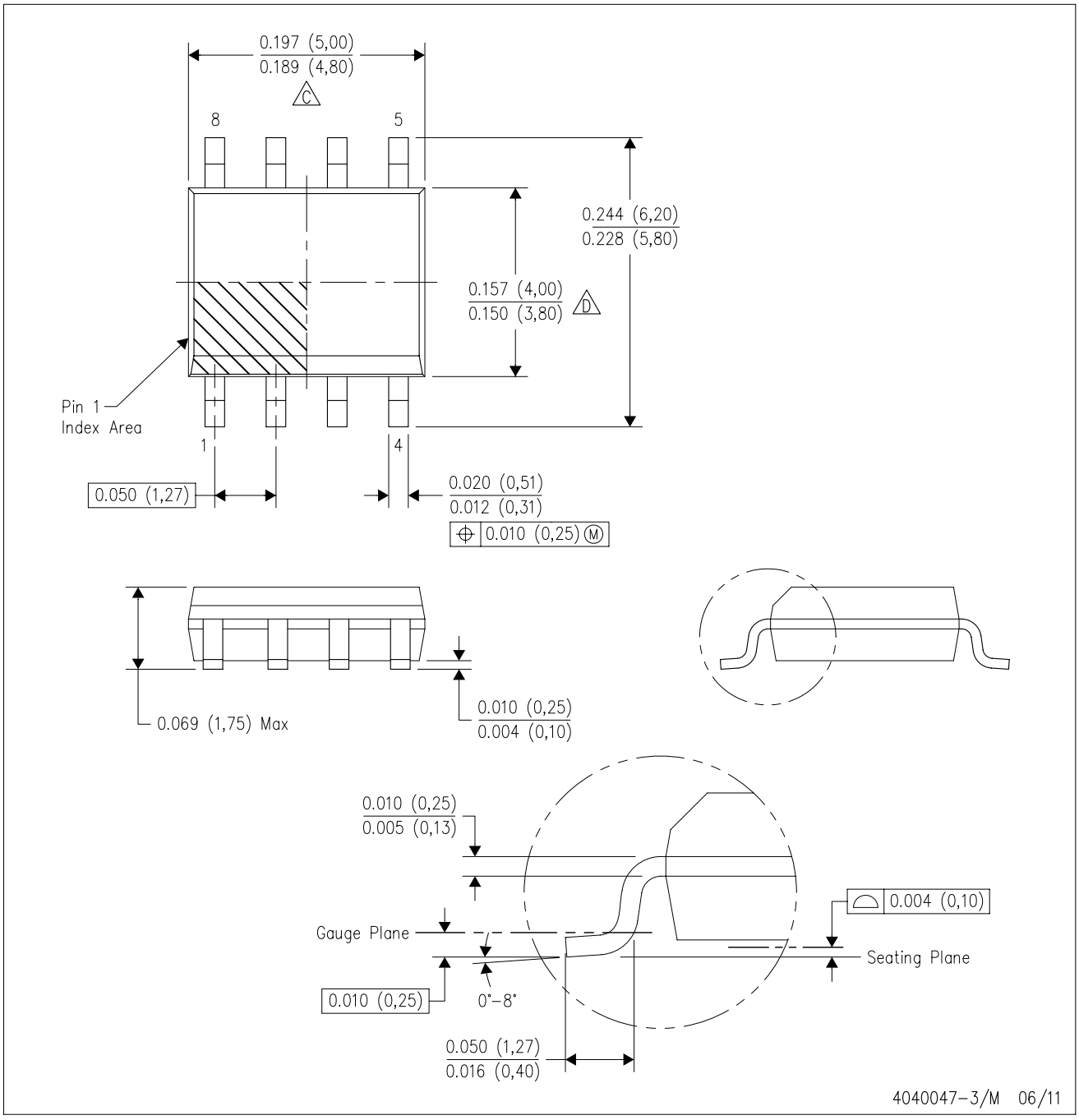
Figure 1. Input Offset-Voltage Null Circuit

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

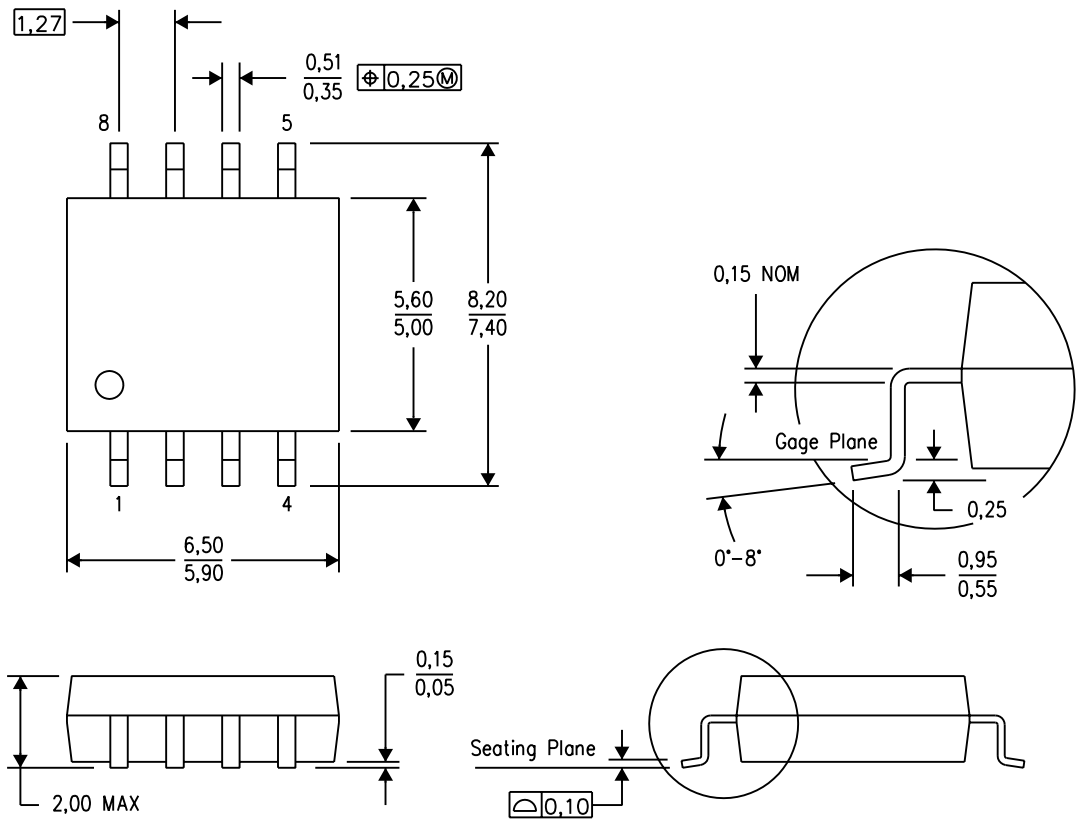
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

MECHANICAL DATA

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.