

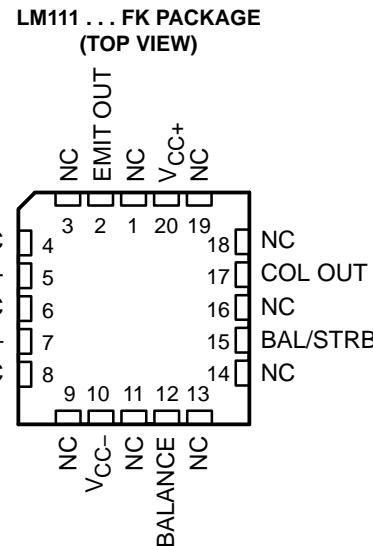
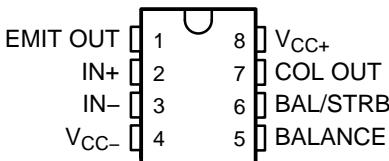
# LM111, LM211, LM311 DIFFERENTIAL COMPARATORS WITH STROBES

SLCS007H – SEPTEMBER 1973 – REVISED AUGUST 2003

- Fast Response Times
- Strobe Capability
- Maximum Input Bias Current . . . 300 nA
- Maximum Input Offset Current . . . 70 nA

- Can Operate From Single 5-V Supply
- Available in Q-Temp Automotive
  - High-Reliability Automotive Applications
  - Configuration Control/Print Support
  - Qualification to Automotive Standards

LM111 . . . JG PACKAGE  
LM211 . . . D, P, OR PW PACKAGE  
LM311 . . . D, P, PS, OR PW PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The LM111, LM211, and LM311 are single high-speed voltage comparators. These devices are designed to operate from a wide range of power-supply voltages, including  $\pm 15\text{-V}$  supplies for operational amplifiers and 5-V supplies for logic systems. The output levels are compatible with most TTL and MOS circuits. These comparators are capable of driving lamps or relays and switching voltages up to 50 V at 50 mA. All inputs and outputs can be isolated from system ground. The outputs can drive loads referenced to ground,  $V_{CC+}$  or  $V_{CC-}$ . Offset balancing and strobe capabilities are available, and the outputs can be wire-OR connected. If the strobe is low, the output is in the off state, regardless of the differential input.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# LM111, LM211, LM311 DIFFERENTIAL COMPARATORS WITH STROBES

SLCS007H – SEPTEMBER 1973 – REVISED AUGUST 2003

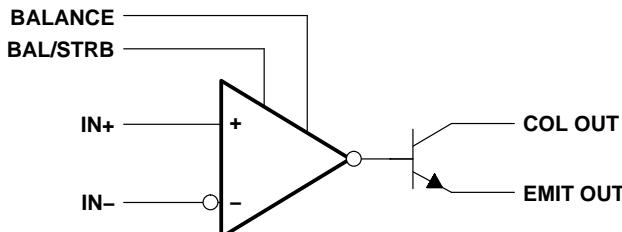
## description/ordering information

### ORDERING INFORMATION

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-0°C to 70°C	7.5 mV	PDIP (P)	Tube of 50	LM311P	LM311P
		SOIC (D)	Tube of 75	LM311D	
			Reel of 2500	LM311DR	LM311
		SOP (PS)	Reel of 2000	LM311PSR	L311
		TSSOP (PW)	Reel of 150	LM311PW	
			Tube of 2000	LM311PWR	L311
-40°C to 85°C	3 mV	PDIP (P)	Tube of 50	LM211P	LM211P
		SOIC (D)	Tube of 75	LM211D	
			Reel of 2500	LM211DR	LM211
		TSSOP (PW)	Reel of 150	LM211PW	
			Reel of 2000	LM211PWR	L211
-40°C to 125°C	3 mV	SOIC (D)	Tube of 75	LM211QD	
			Reel of 2500	LM211QDR	LM211Q
-55°C to 125°C	3 mV	CDIP (JG)	Tube of 50	LM111JG	LM111JG
		LCCC (FK)	Tube of 55	LM111FK	LM111FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

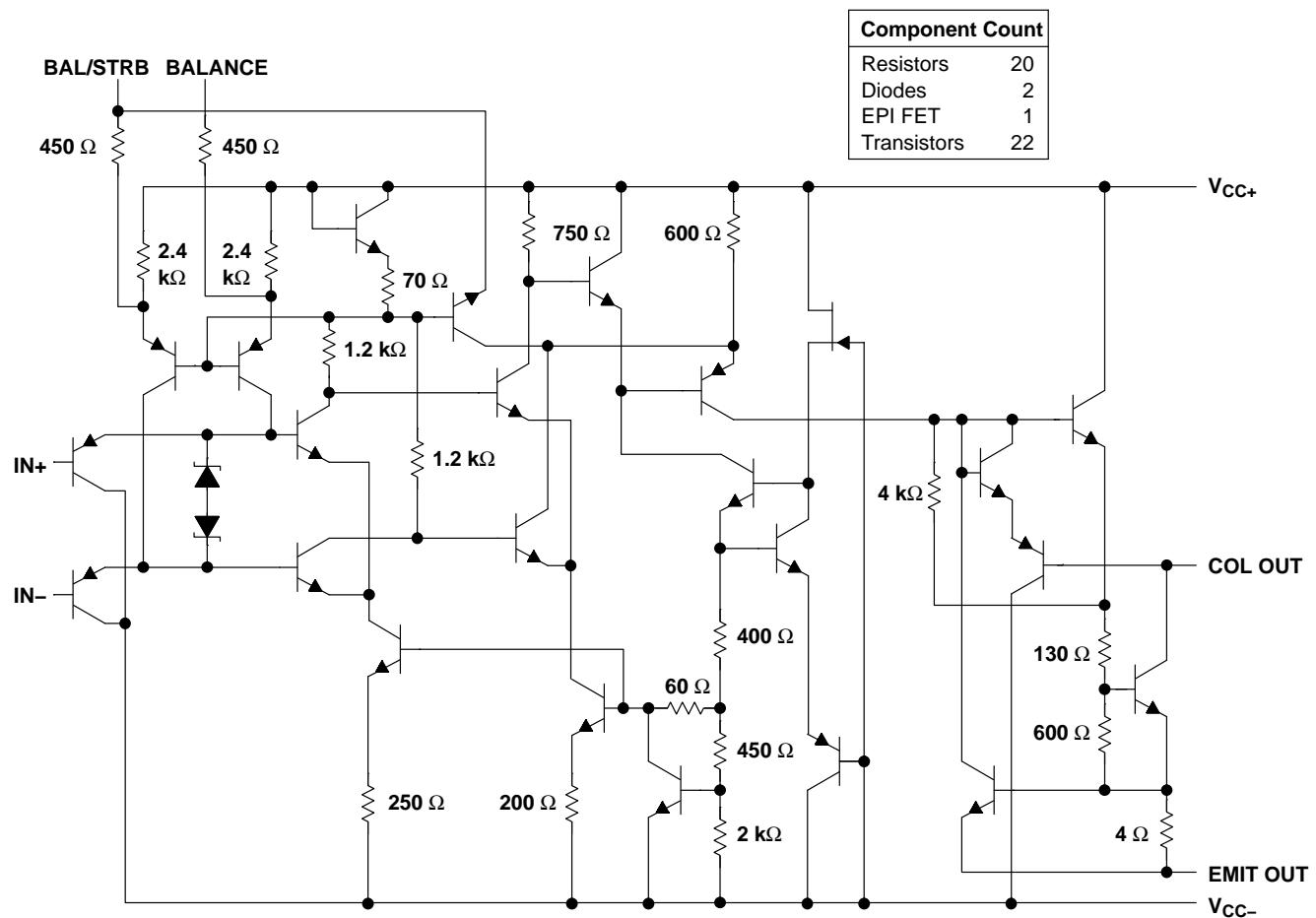
## functional block diagram



# LM111, LM211, LM311 DIFFERENTIAL COMPARATORS WITH STROBES

SLCS007H – SEPTEMBER 1973 – REVISED AUGUST 2003

## schematic



All resistor values shown are nominal.

# LM111, LM211, LM311 DIFFERENTIAL COMPARATORS WITH STROBES

SLCS007H – SEPTEMBER 1973 – REVISED AUGUST 2003

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage: $V_{CC+}$ (see Note 1) .....	18 V
$V_{CC-}$ (see Note 1) .....	-18 V
$V_{CC+} - V_{CC-}$ .....	36 V
Differential input voltage, $V_{ID}$ (see Note 2) .....	$\pm 30$ V
Input voltage, $V_I$ (either input, see Notes 1 and 3) .....	$\pm 15$ V
Voltage from emitter output to $V_{CC-}$ .....	30 V
Voltage from collector output to $V_{CC-}$ :	
LM111 .....	50 V
LM211 .....	50 V
LM211Q .....	50 V
LM311 .....	40 V
Duration of output short circuit (see Note 4) .....	10 s
Package thermal impedance, $\theta_{JA}$ (see Notes 5 and 6):	
D package .....	97°C/W
P package .....	85°C/W
PS package .....	95°C/W
PW package .....	149°C/W
Package thermal impedance, $\theta_{JC}$ (see Notes 7 and 8):	
FK package .....	5.61°C/W
JG package .....	14.5°C/W
Operating virtual junction temperature, $T_J$ .....	150°C
Case temperature for 60 seconds: FK package .....	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J or JG package .....	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, P, PS, or PW package .....	260°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .

2. Differential voltages are at IN+ with respect to IN-.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or  $\pm 15$  V, whichever is less.
4. The output may be shorted to ground or either power supply.
5. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JEDEC 51-7.
7. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JC}$ , and  $T_C$ . The maximum allowable power dissipation at any allowable case temperature is  $P_D = (T_J(max) - T_C)/\theta_{JC}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
8. The package thermal impedance is calculated in accordance with MIL-STD-883.

## recommended operating conditions

		MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage	3.5	30	V
$V_I$	Input voltage ( $ V_{CC\pm}  \leq 15$ V)	$V_{CC-} + 0.5$	$V_{CC+} - 1.5$	V
$T_A$	Operating free-air temperature range	LM111	-55	125
		LM211	-40	85
		LM211Q	-40	125
		LM311	0	70

LM111, LM211, LM311  
DIFFERENTIAL COMPARATORS WITH STROBES

SLCS007H – SEPTEMBER 1973 – REVISED AUGUST 2003

**electrical characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 15$  V (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	LM111 LM211 LM211Q			LM311			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IO}$ Input offset voltage	See Note 6	25°C	0.7	3	2	7.5			mV
		Full range		4		10		10	
$I_{IO}$ Input offset current	See Note 6	25°C	4	10	6	50			nA
		Full range		20		70			
$I_{IB}$ Input bias current	$V_O = 1$ V to 14 V	25°C	75	100	100	250			nA
		Full range		150		300			
$I_{IL(S)}$ Low-level strobe current (see Note 7)	$V_{(strobe)} = 0.3$ V, $V_{ID} \leq -10$ mV	25°C		-3		-3			mA
$V_{ICR}$ Common-mode input voltage range		Full range	13 to -14.5	13.8 to -14.7		13 to -14.5	13.8 to -14.7		V
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 5$ V to 35 V, $R_L = 1$ kΩ	25°C	40	200	40	200			V/mV
$I_{OH}$ High-level (collector) output leakage current	$I_{(strobe)} = -3$ mA, $V_{OH} = 35$ V, $V_{ID} = 5$ mV	25°C	0.2	10					nA
		Full range		0.5					µA
	$V_{ID} = 5$ mV, $V_{OH} = 35$ V	25°C				0.2	50		nA
$V_{OL}$ Low-level (collector-to-emitter) output voltage	$I_{OL} = 50$ mA	$V_{ID} = -5$ mV	25°C	0.75	1.5				V
		$V_{ID} = -10$ mV	25°C			0.75	1.5		
	$V_{CC+} = 4.5$ V, $V_{CC-} = 0$ , $I_{OL} = 8$ mA	$V_{ID} = -6$ mV	Full range	0.23	0.4				V
		$V_{ID} = -10$ mV	Full range			0.23	0.4		
$I_{CC+}$ Supply current from $V_{CC+}$ , output low	$V_{ID} = -10$ mV, No load	25°C	5.1	6	5.1	7.5			mA
$I_{CC-}$ Supply current from $V_{CC-}$ , output high	$V_{ID} = 10$ mV, No load	25°C	-4.1	-5	-4.1	-5			mA

† Unless otherwise noted, all characteristics are measured with BALANCE and BAL/STRB open and EMIT OUT grounded.

Full range for LM111 is -55°C to 125°C, for LM211 is -40°C to 85°C, for LM211Q is -40°C to 125°C, and for LM311 is 0°C to 70°C.

‡ All typical values are at  $T_A = 25^\circ\text{C}$ .

NOTES: 9. The offset voltages and offset currents given are the maximum values required to drive the collector output up to 14 V or down to 1 V with a pullup resistor of 7.5 kΩ to  $V_{CC+}$ . These parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

10. The strobe should not be shorted to ground; it should be current driven at -3 mA to -5 mA (see Figures 13 and 27).

**switching characteristics,  $V_{CC\pm} = \pm 15$  V,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	LM111 LM211 LM211Q LM311		UNIT
		TYP		
Response time, low-to-high-level output	$R_C = 500$ Ω to 5 V, $C_L = 5$ pF, See Note 8	115		ns
Response time, high-to-low-level output		165		ns

NOTE 11: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# LM111, LM211, LM311 DIFFERENTIAL COMPARATORS WITH STROBES

SLCS007H – SEPTEMBER 1973 – REVISED AUGUST 2003

## TYPICAL CHARACTERISTICS<sup>†</sup>

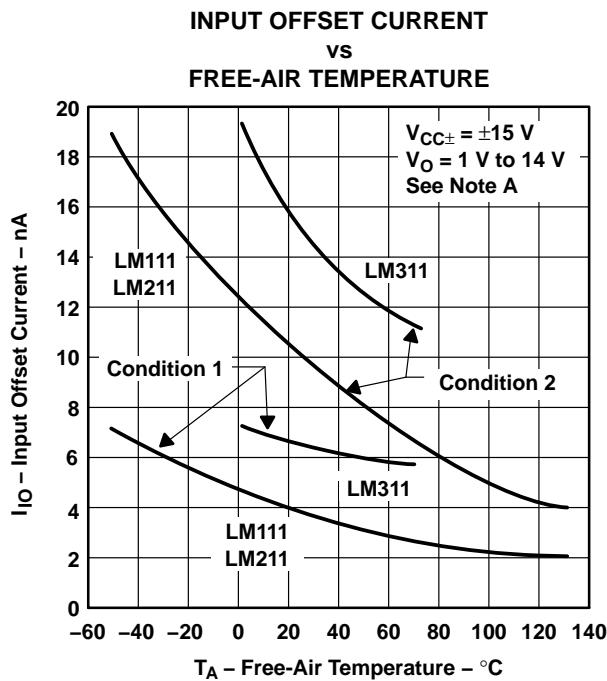


Figure 1

NOTE A: Condition 1 is with BALANCE and BAL/STRB open.  
Condition 2 is with BALANCE and BAL/STRB connected to  $V_{CC+}$ .

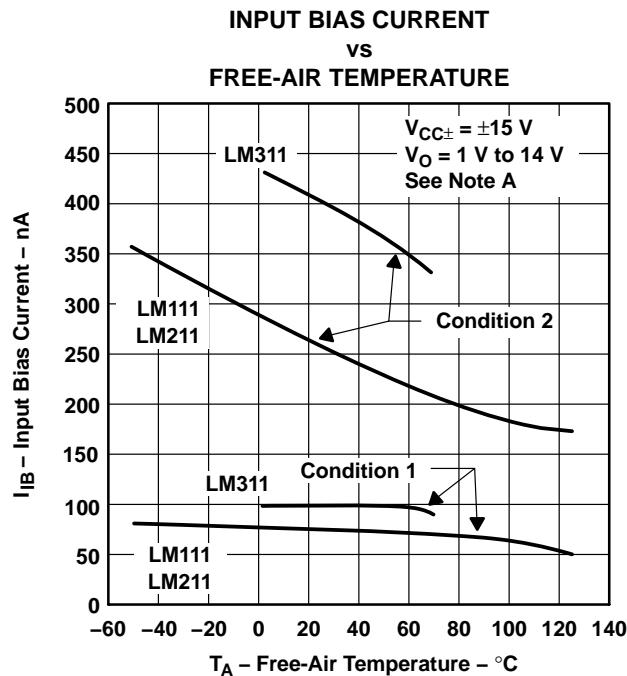


Figure 2

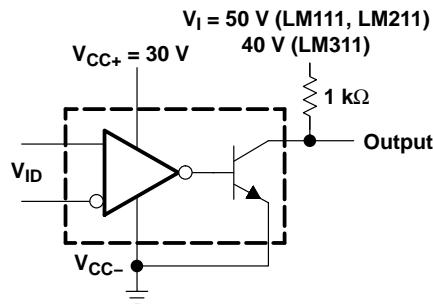
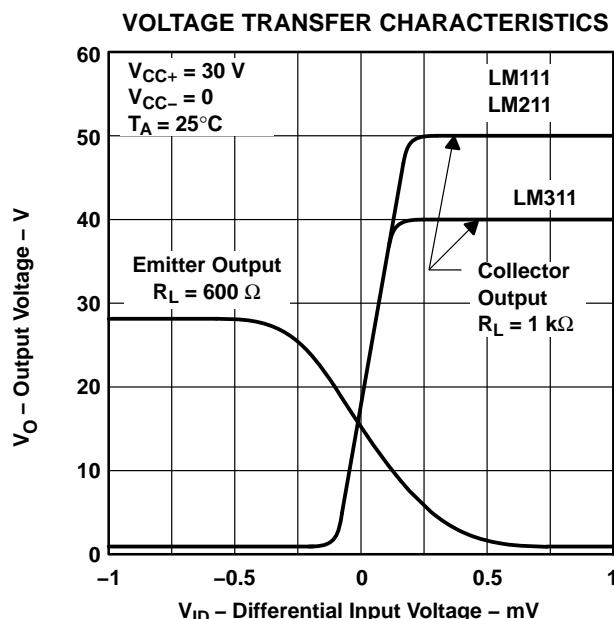
NOTE A: Condition 1 is with BALANCE and BAL/STRB open.  
Condition 2 is with BALANCE and BAL/STRB connected to  $V_{CC+}$ .

<sup>†</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

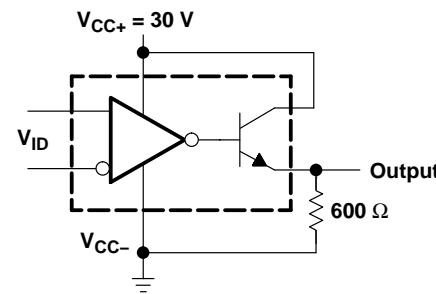
# LM111, LM211, LM311 DIFFERENTIAL COMPARATORS WITH STROBES

SLCS007H – SEPTEMBER 1973 – REVISED AUGUST 2003

## TYPICAL CHARACTERISTICS<sup>†</sup>



**COLLECTOR OUTPUT TRANSFER CHARACTERISTIC TEST CIRCUIT FOR FIGURE 3**



**EMITTER OUTPUT TRANSFER CHARACTERISTIC TEST CIRCUIT FOR FIGURE 3**

**Figure 3**

<sup>†</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

# LM111, LM211, LM311 DIFFERENTIAL COMPARATORS WITH STROBES

SLCS007H – SEPTEMBER 1973 – REVISED AUGUST 2003

## TYPICAL CHARACTERISTICS

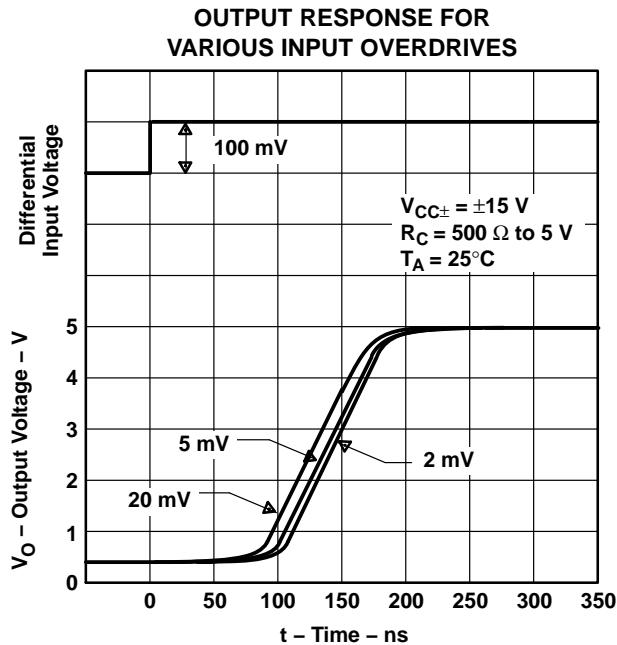


Figure 4

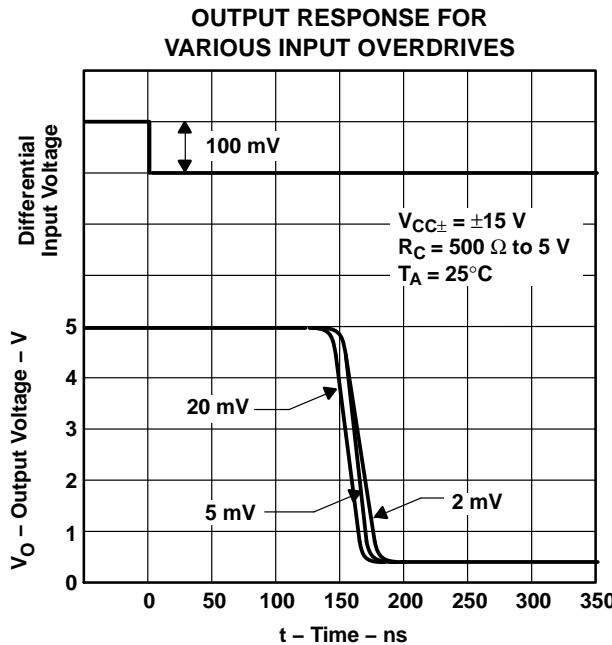
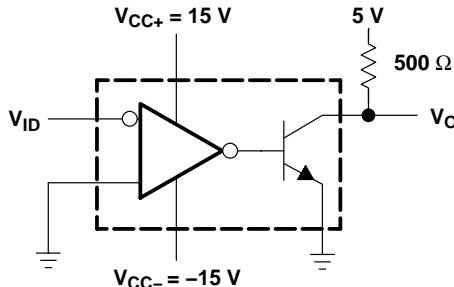
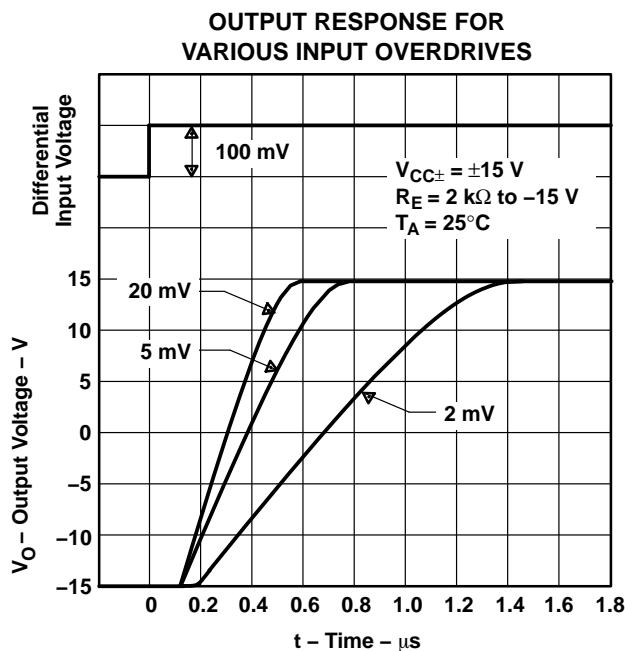


Figure 5

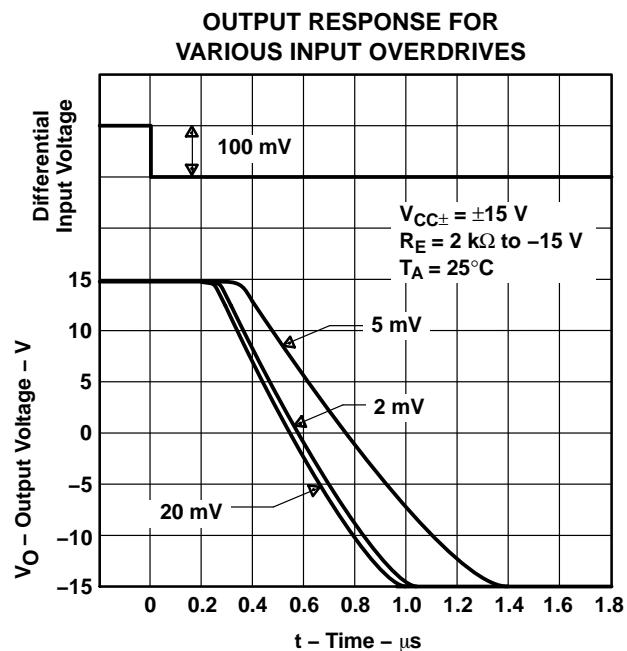


TEST CIRCUIT FOR FIGURES 4 AND 5

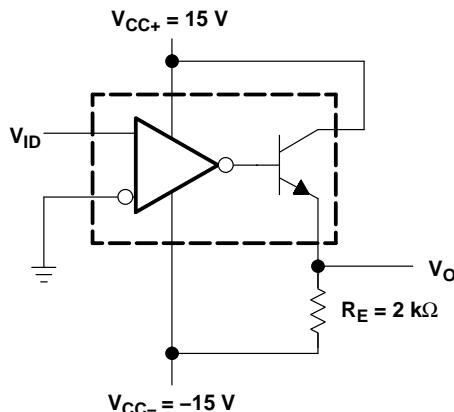
### TYPICAL CHARACTERISTICS



**Figure 6**



**Figure 7**



**TEST CIRCUIT FOR FIGURES 6 AND 7**

# LM111, LM211, LM311 DIFFERENTIAL COMPARATORS WITH STROBES

SLCS007H – SEPTEMBER 1973 – REVISED AUGUST 2003

## TYPICAL CHARACTERISTICS

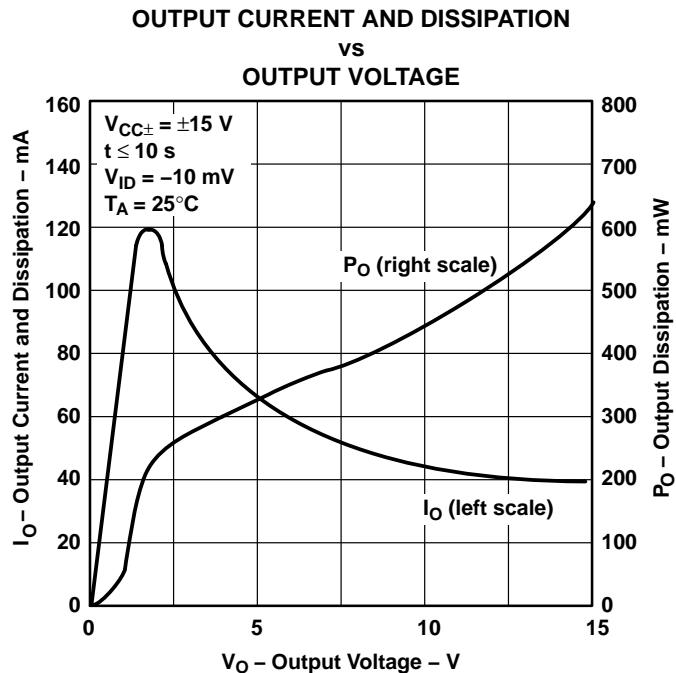


Figure 8

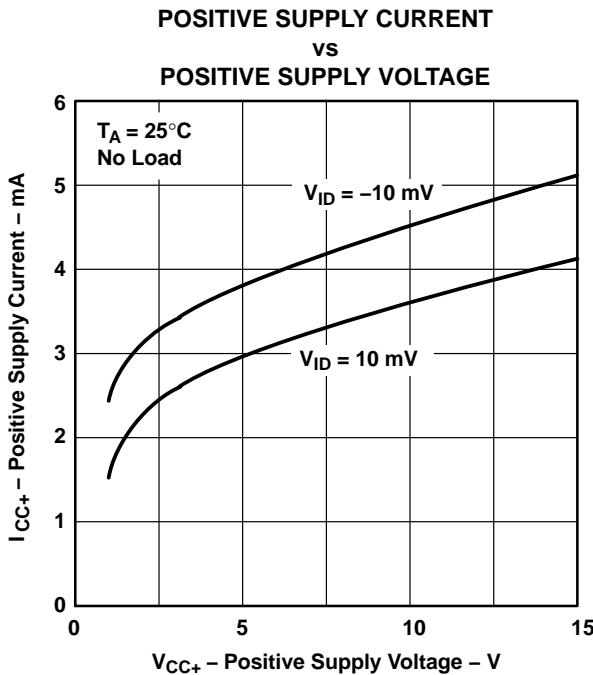


Figure 9

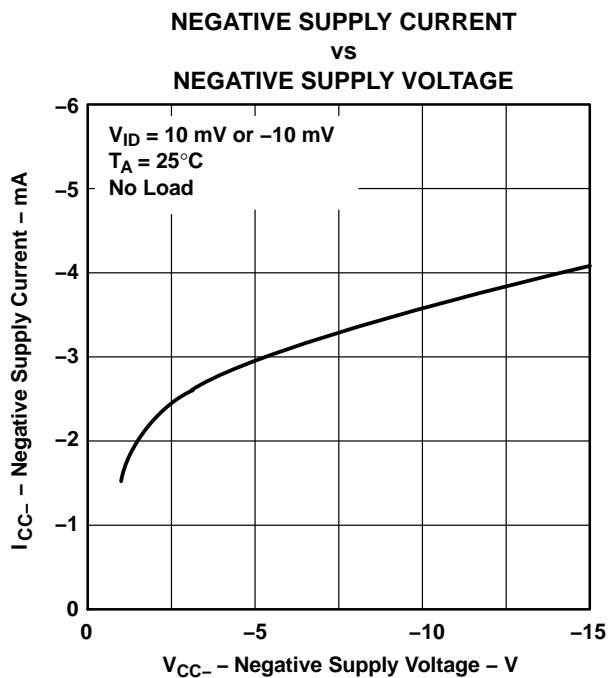
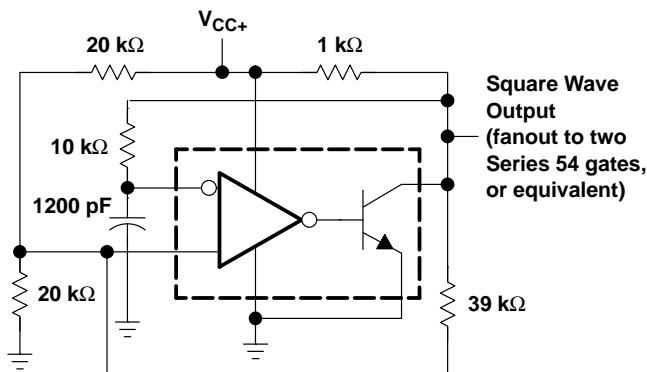


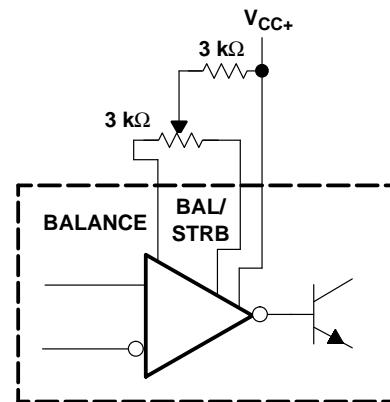
Figure 10

## APPLICATION INFORMATION

Figure 11 through Figure 29 show various applications for the LM111, LM211, and LM311 comparators.

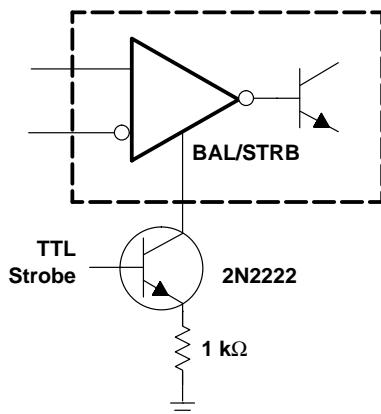


**Figure 11. 100-kHz Free-Running Multivibrator**



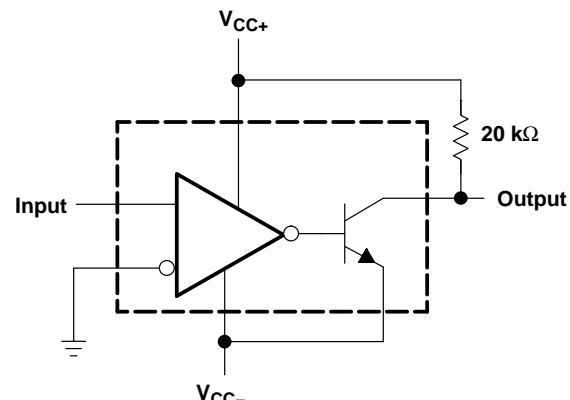
NOTE: If offset balancing is not used, the BALANCE and BAL/STRB pins should be shorted together.

**Figure 12. Offset Balancing**



**Figure 13. Strobing**

NOTE: Do not connect strobe pin directly to ground, because the output is turned off whenever current is pulled from the strobe pin.

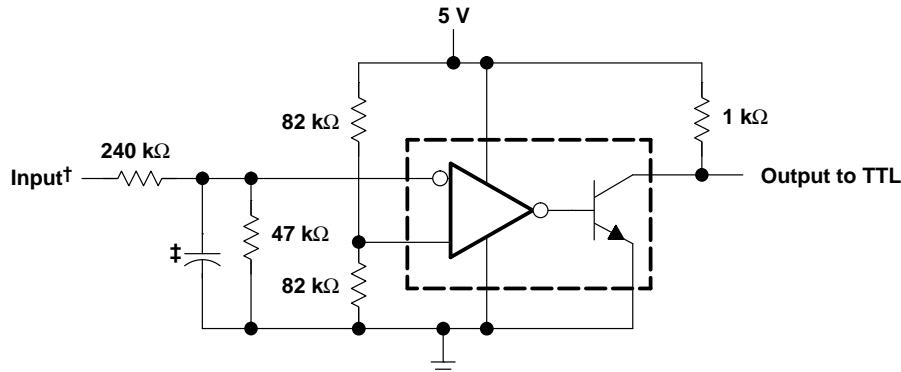


**Figure 14. Zero-Crossing Detector**

# LM111, LM211, LM311 DIFFERENTIAL COMPARATORS WITH STROBES

SLCS007H – SEPTEMBER 1973 – REVISED AUGUST 2003

## APPLICATION INFORMATION



† Resistor values shown are for a 0- to 30-V logic swing and a 15-V threshold.

‡ May be added to control speed and reduce susceptibility to noise spikes

Figure 15. TTL Interface With High-Level Logic

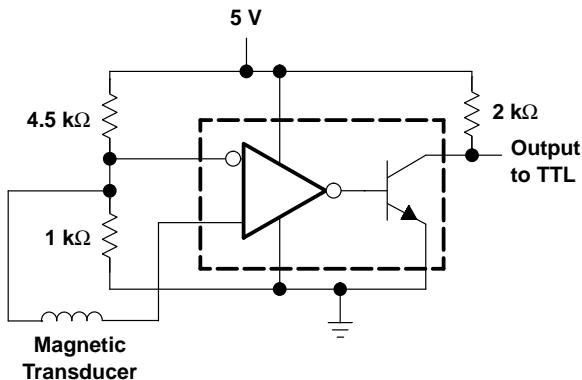


Figure 16. Detector for Magnetic Transducer

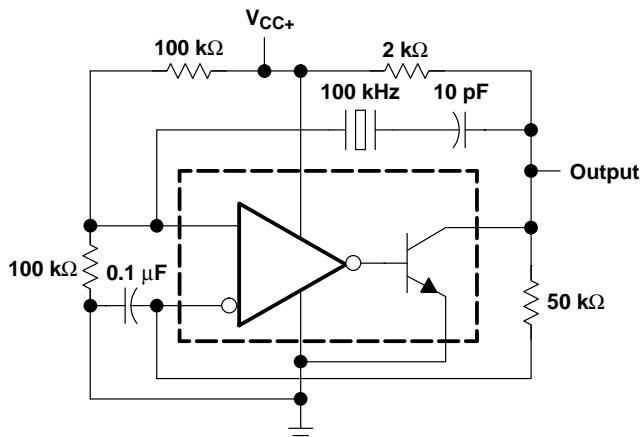
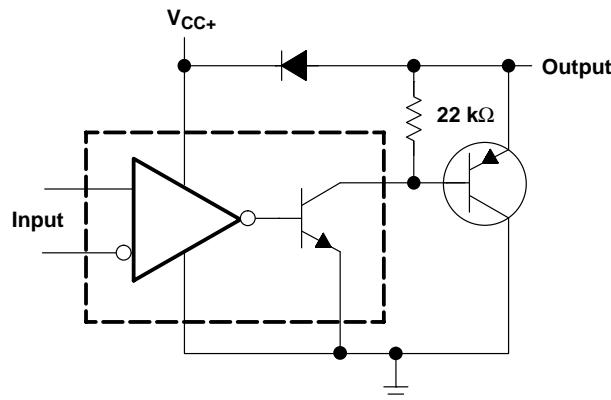
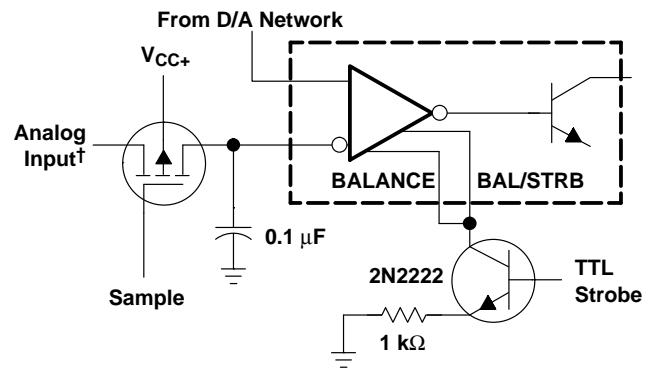


Figure 17. 100-kHz Crystal Oscillator

## APPLICATION INFORMATION

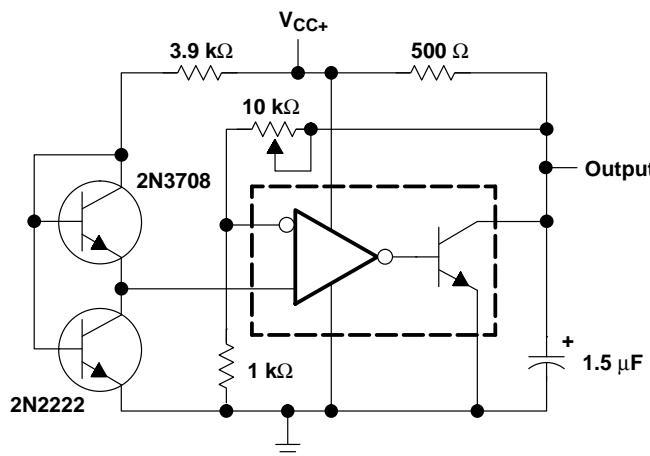


**Figure 18. Comparator and Solenoid Driver**

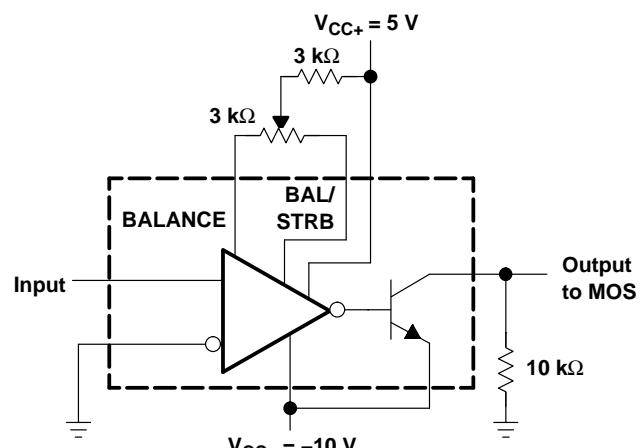


† Typical input current is 50 pA with inputs strobed off.

**Figure 19. Strobing Both Input and Output Stages Simultaneously**



**Figure 20. Low-Voltage Adjustable Reference Supply**

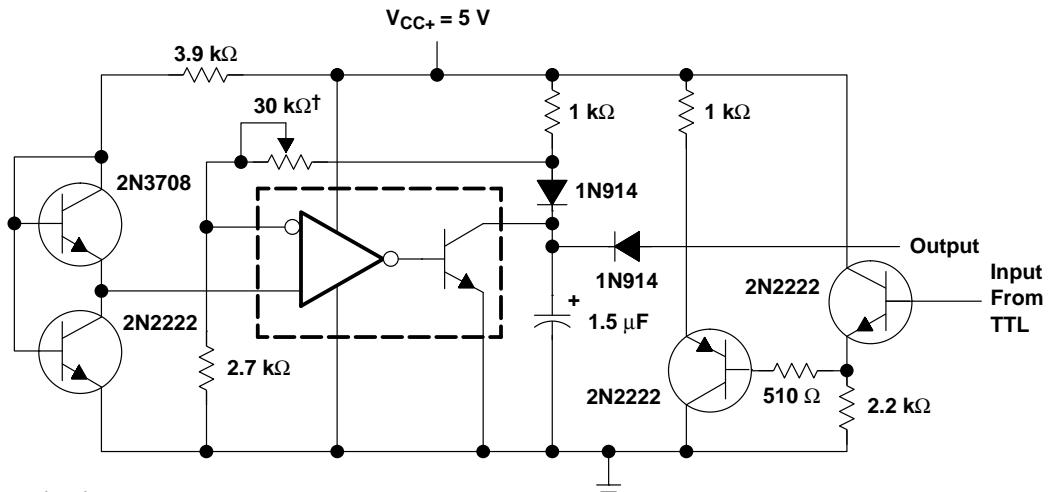


**Figure 21. Zero-Crossing Detector Driving MOS Logic**

# LM111, LM211, LM311 DIFFERENTIAL COMPARATORS WITH STROBES

SLCS007H – SEPTEMBER 1973 – REVISED AUGUST 2003

## APPLICATION INFORMATION



<sup>†</sup> Adjust to set clamp level

Figure 22. Precision Squarer

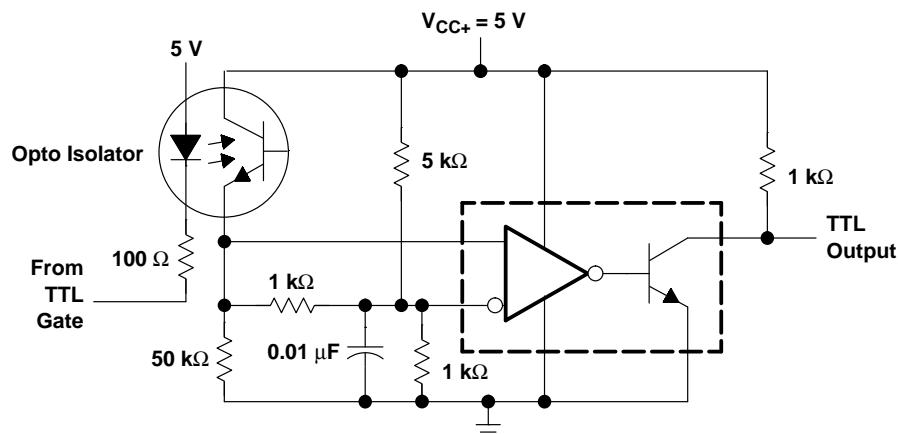


Figure 23. Digital Transmission Isolator

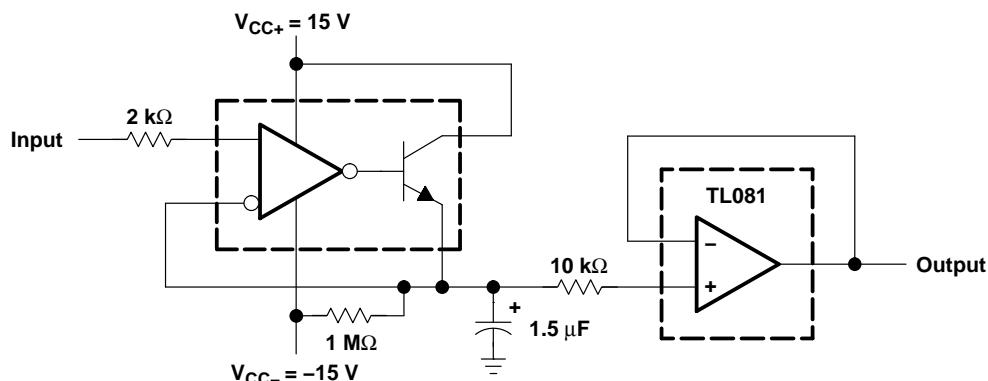
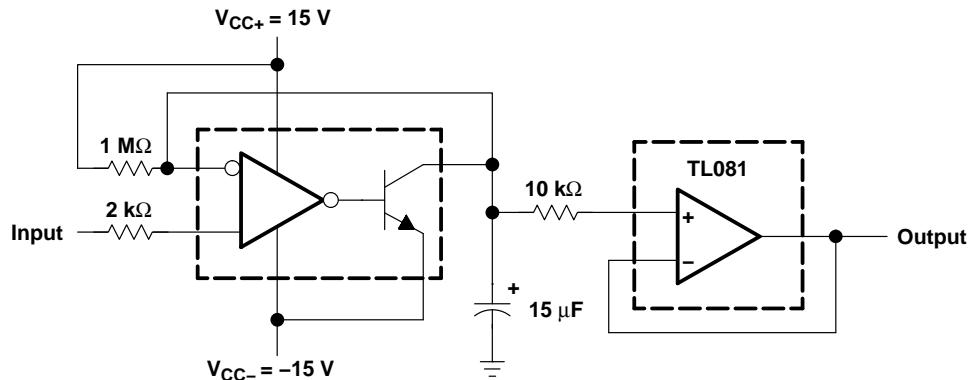


Figure 24. Positive-Peak Detector

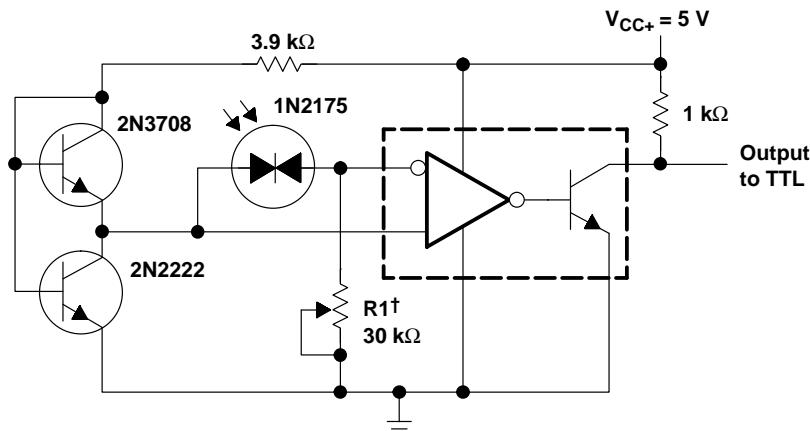


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

### APPLICATION INFORMATION

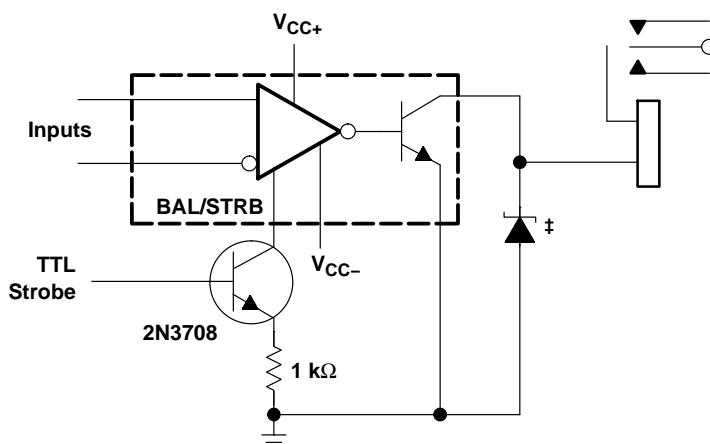


**Figure 25. Negative-Peak Detector**



† R1 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing dark current by an order of magnitude.

**Figure 26. Precision Photodiode Comparator**



‡ Transient voltage and inductive kickback protection

**Figure 27. Relay Driver With Strobe**

# LM111, LM211, LM311 DIFFERENTIAL COMPARATORS WITH STROBES

SLCS007H – SEPTEMBER 1973 – REVISED AUGUST 2003

## APPLICATION INFORMATION

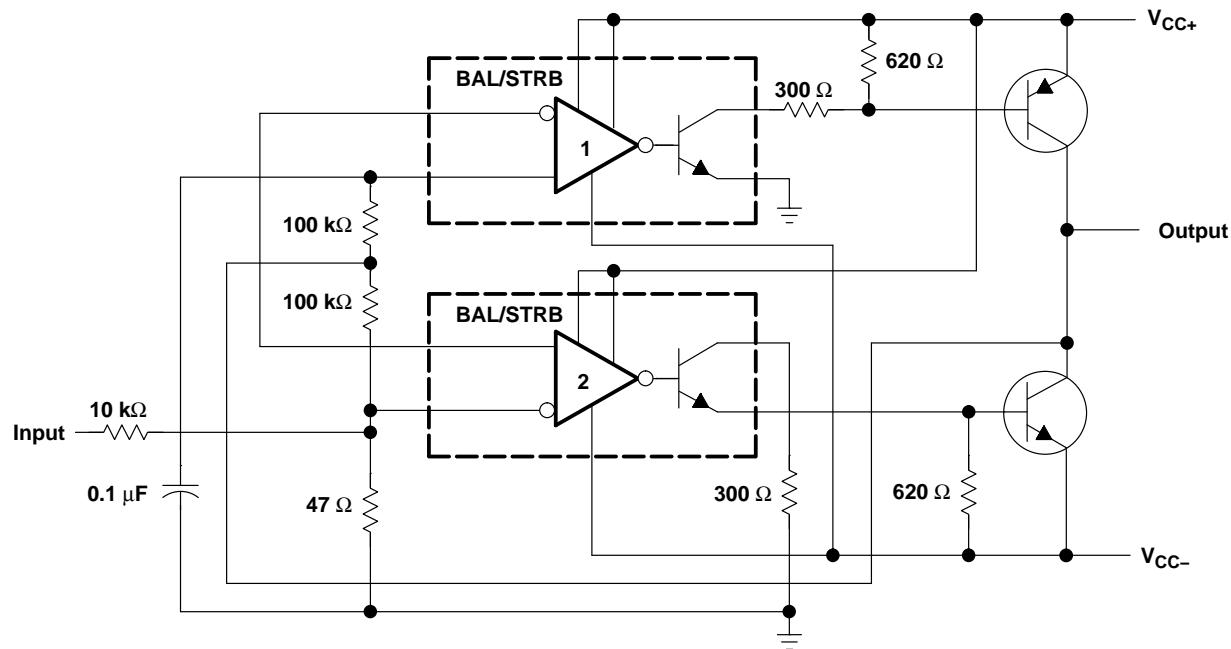


Figure 28. Switching Power Amplifier

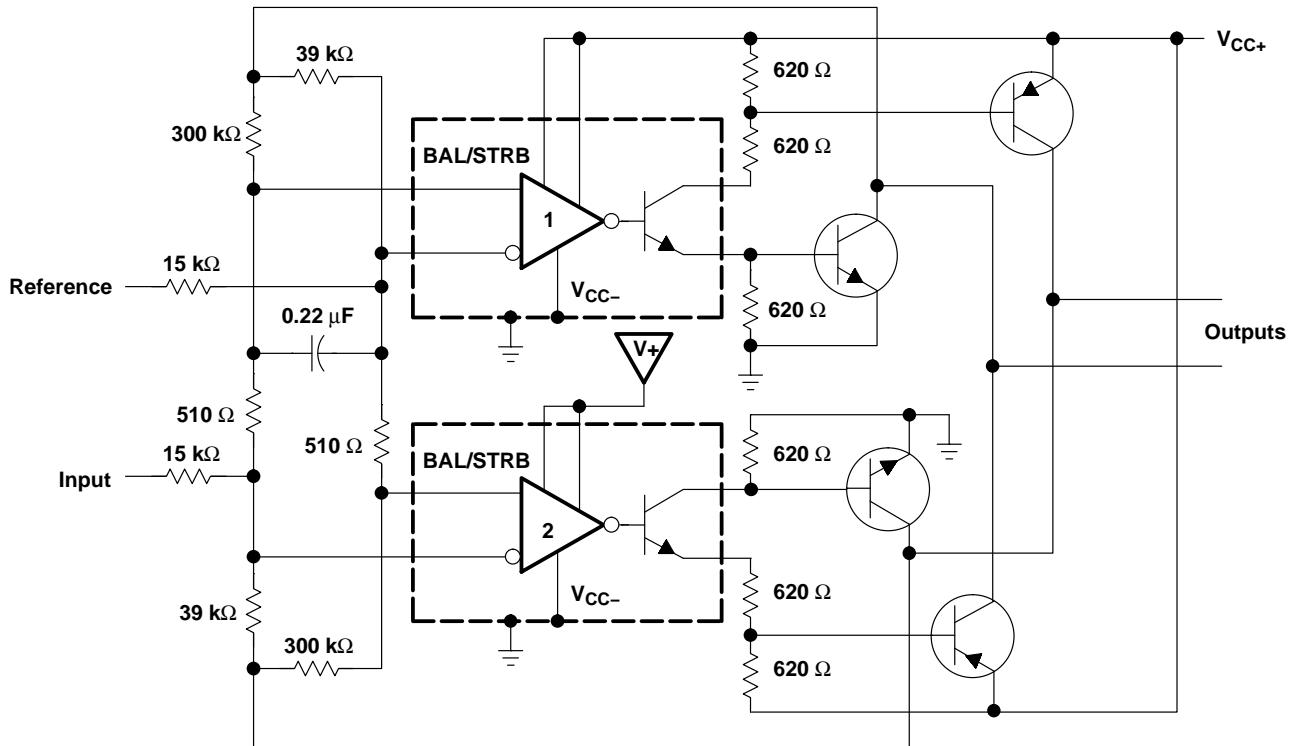


Figure 29. Switching Power Amplifiers

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	
LM211PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	L211	
LM211QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM211Q	
LM211QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM211Q	
LM211QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM211Q	
LM211QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM211Q	
LM311D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	
LM311DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	
LM311DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	
LM311DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	
LM311DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	
LM311DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM311	
LM311P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LM311P	
LM311PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LM311P	
LM311PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	
LM311PSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	
LM311PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	
LM311PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	
LM311PWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L311	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)
LM311PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L311
LM311PWLE	OBsolete	TSSOP	PW	8		TBD	Call TI	Call TI		
LM311PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L311
LM311PWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L311
LM311PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L311
LM311Y	OBsolete	DIESALE	Y	0		TBD	Call TI	Call TI		
M38510/10304BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /10304BPA

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

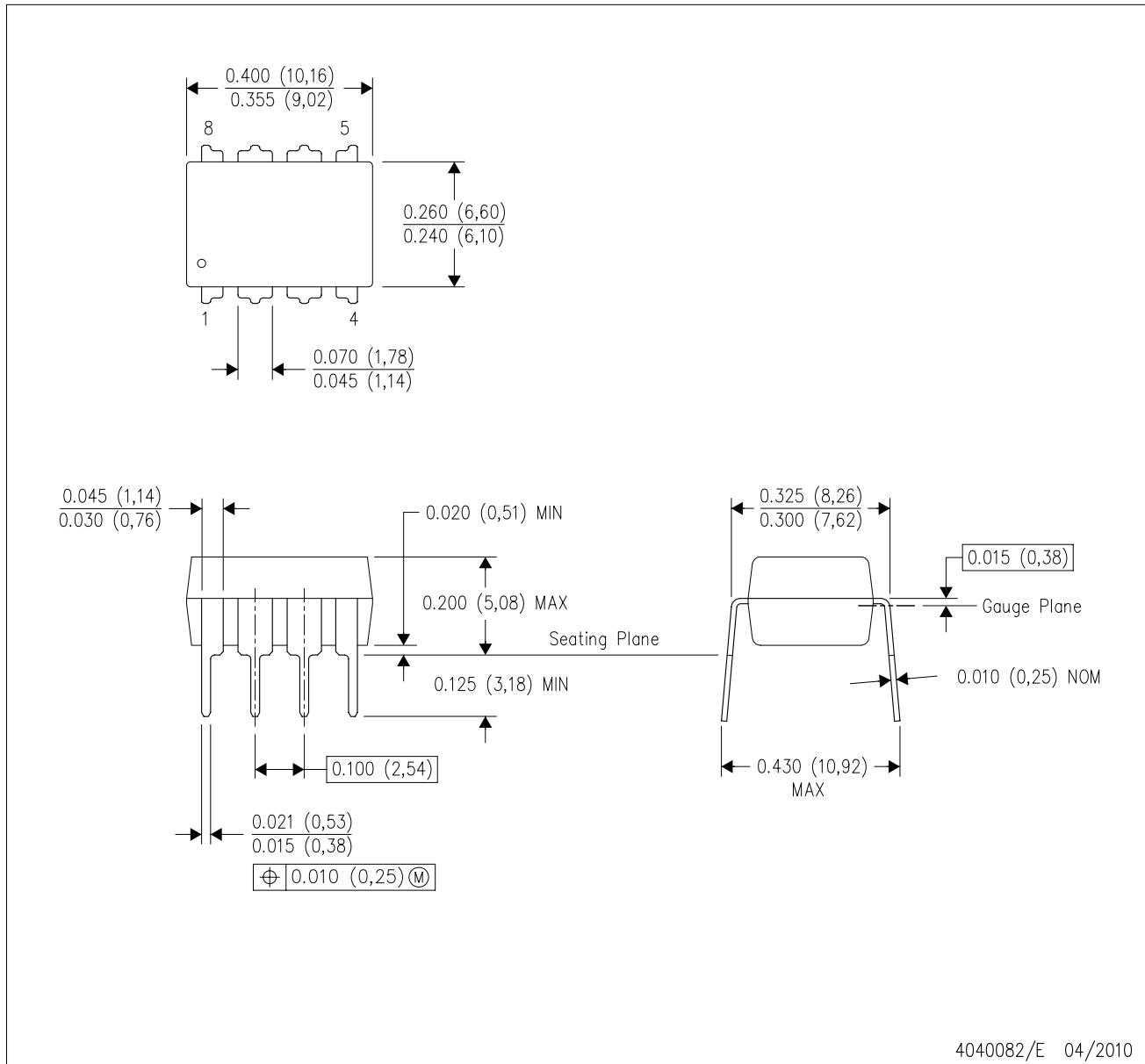
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

## MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

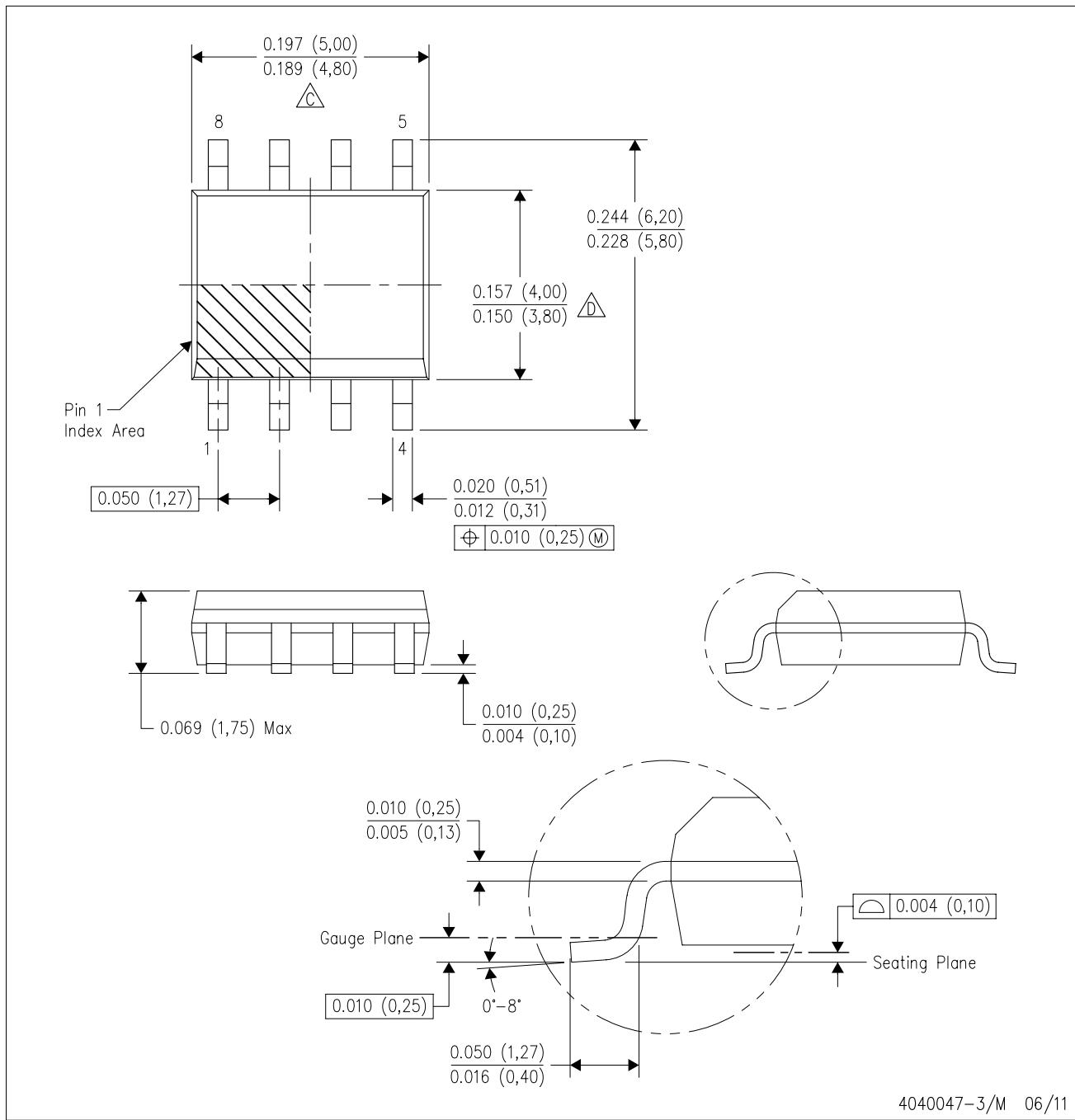


4040082/E 04/2010

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

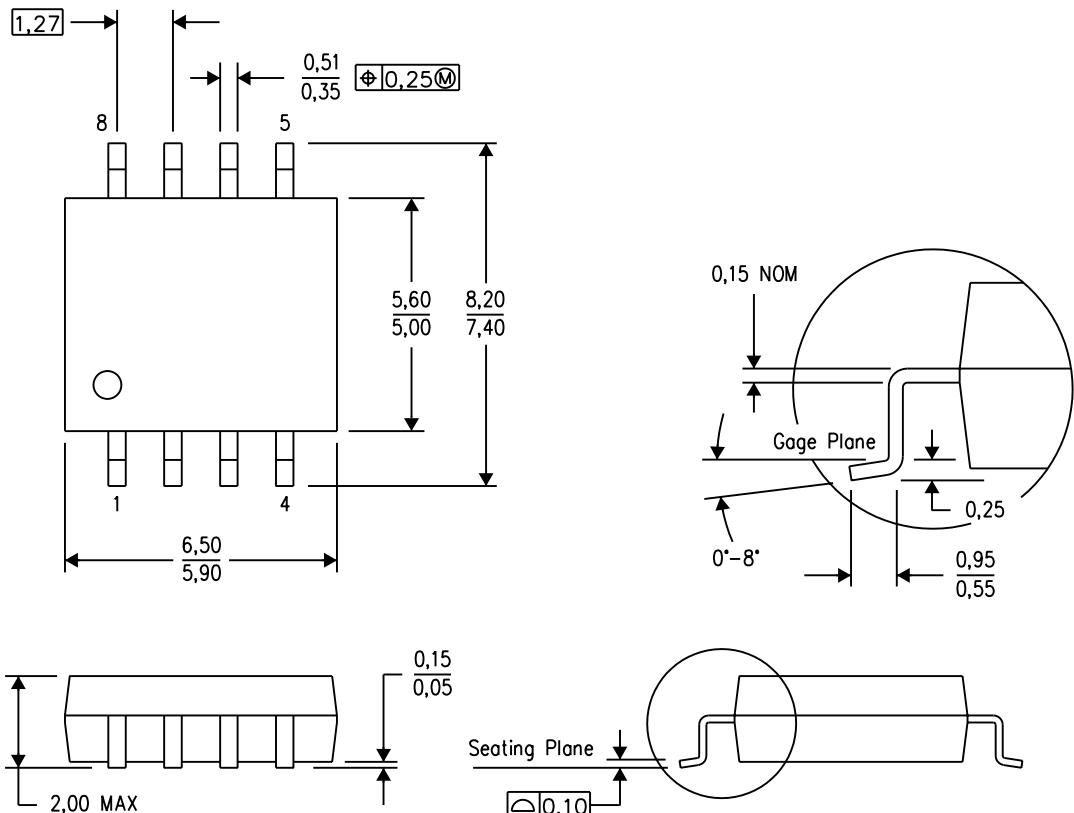
E. Reference JEDEC MS-012 variation AA.

---

## MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



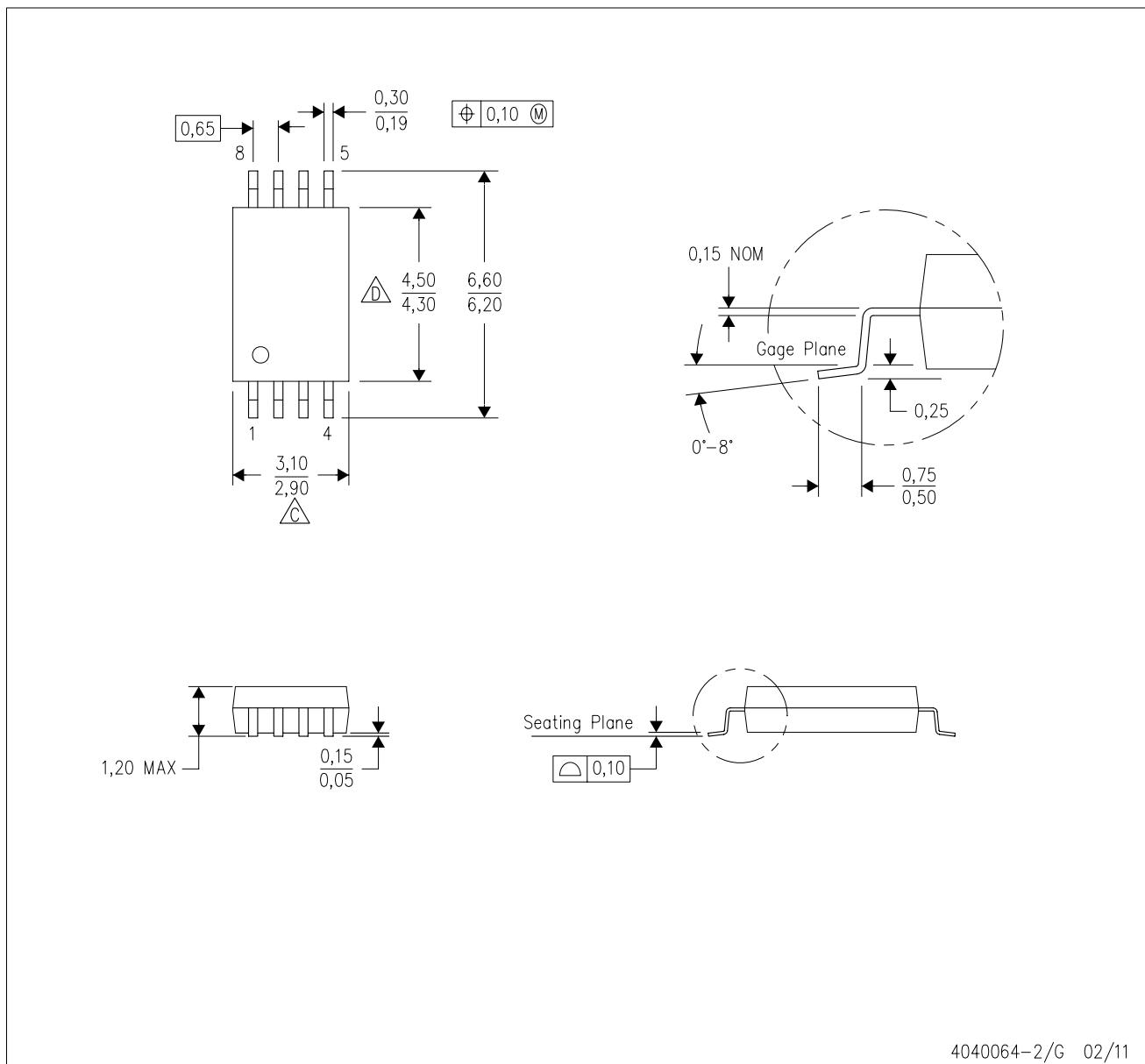
4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## MECHANICAL DATA

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040064-2/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153